

COMPAL CONFIDENTIAL

MODEL NAME : **VAQ10**

PCB NO : **LA-9771P**

BOM P/N : **4319MF31L01(TPM HDMI LVDS)**
4319MF31L02(TPM HDMI QHD)
4319MF31L03(DTP HDMI LVDS)
4319MF31L04(DTP HDMI QHD)

GPIO MAP:

Diesel 15"

REV : 0.2 (X01)

2013.XX.XX

1@ : LVDS panel

2@ : eDP(QHD) panel

EMC@ : EMI/ESD/RF part

@ : Nopop Component

CONN@ : Connector Component

CXDP@,PXDP@ : Total debug Component (pop them until ST)

MB PCB

Part Number	Description
DAA00061000	PCB 0MF LA-9771P REV0 MB

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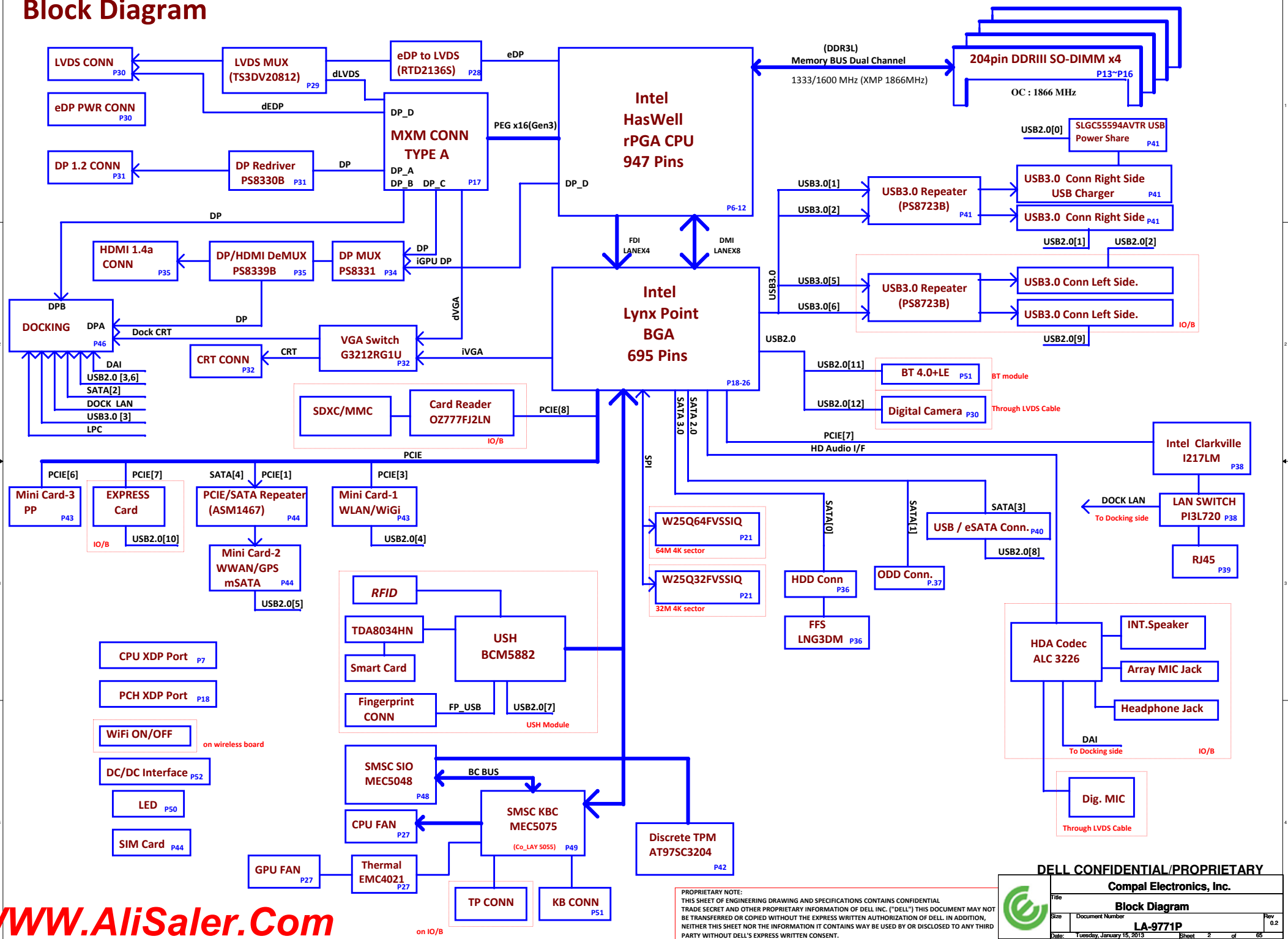


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Block Diagram



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW2 +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +VCC_CORE +1.05V_RUN	+3.3V_M +1.05V_M (M-OFF)	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50
			Add Plating		1.00
1	Top		Copper foil	0.5oz	0.65
2	GND1	3.7	Prepreg	1080	2.50
			Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
3	Sig 1		Copper foil	1oz	1.35
		4.1	Prepreg	2116Mx2	8.26
4	GND/PWR		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
5	Sig 2		Copper foil	1oz	1.35
		3.8	Prepreg	1080Hx2	4.60
6	Sig 3		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
7	GND/PWR		Copper foil	1oz	1.35
		4.1	Prepreg	2116Mx2	8.26
8	Sig 4		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
9	GND 3		Copper foil	1oz	1.35
		3.7	Prepreg	1080	2.50
10	Bottom		Copper foil	0.5oz	0.65
			Add Plating		1.00
			SolderMask		0.50
Overall Thickness (1.45mm ± 10%)				57.09	57.26000
					1.454404

SATA	DESTINATION
SATA 0	HDD1
SATA 1	ODD
SATA 2	Dock
SATA 3	ESATA
SATA 4	mSATA
SATA 5	NA

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side)
	1	JUSB2 (Ext Right Side)
	2	IO Board- JUSB1 (Ext Left Side)
	3	Docking USB3.0
	4	WLAN/WIGIG
	5	WWAN/GPS/LTE/UWB/mSATA
	6	Docking USB 2.0
	7	USH
	8	ESATA
	9	IO Board- JUSB2 (Ext Left Side)
	10	Express Card
	11	NA
USH	12	Carmera
	13	NA
USH	0	BIO
	1	NA

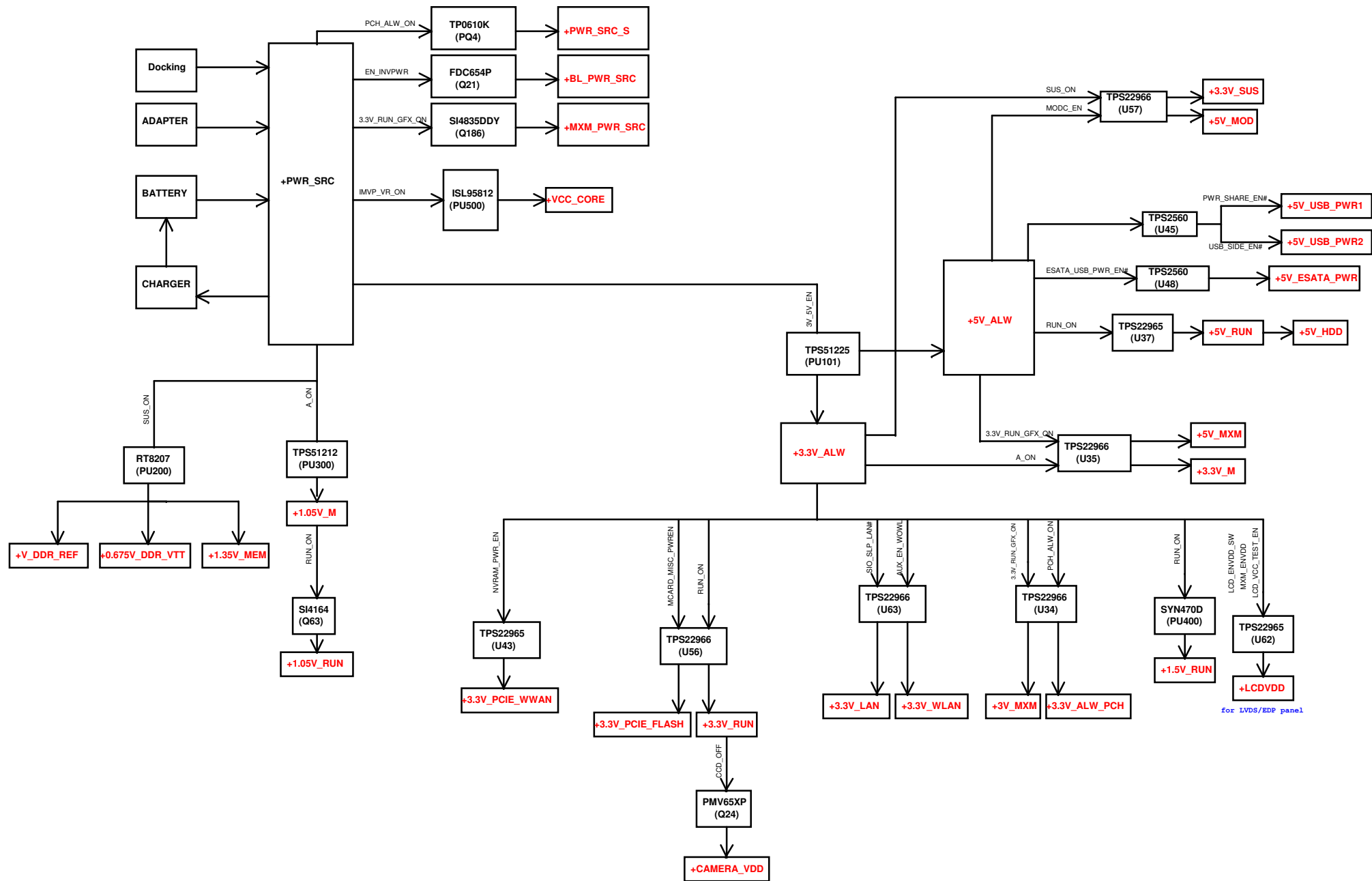
PCI EXPRESS	DESTINATION
Lane 1	mSATA/WWAN
Lane 2	10/100/1G LOM
Lane 3	MINI CARD-2 (WLAN)
Lane 4	NA
Lane 5	NA
Lane 6	NA
Lane 7	EXPRESS CARD
Lane 8	MMI(Card reader)

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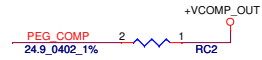


Power Rail
LA-9771P

Rev 0.2

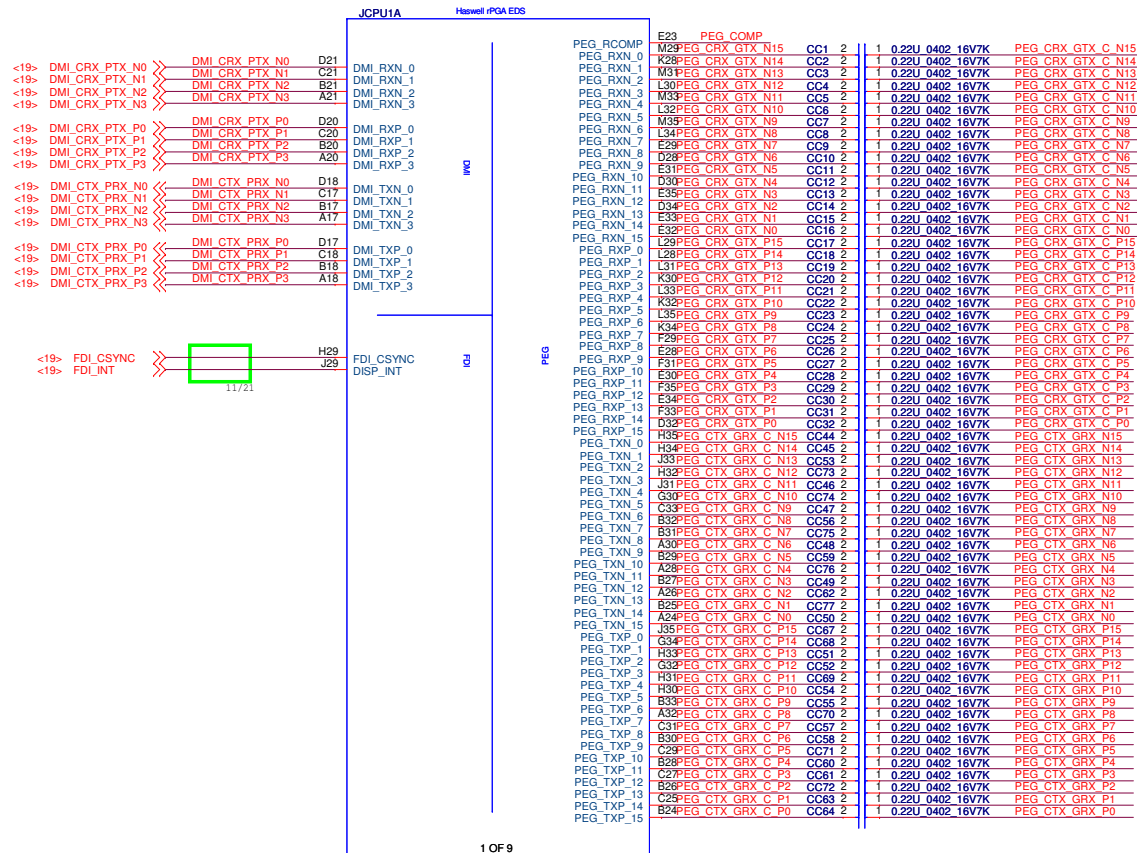
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CAD Note:
Trace width=12 mils ,Spacing=15mil
Max length= 400 mils.

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PEG_CRX_GTX_C_N[0..15] <<PEG_CRX_GTX_C_N[0..15] <17>
PEG_CTX_GRX_P[0..15] >>PEG_CTX_GRX_P[0..15] <17>
PEG_CTX_GRX_N[0..15] >>PEG_CTX_GRX_N[0..15] <17>



CONN@
CPU socket Reverse type.

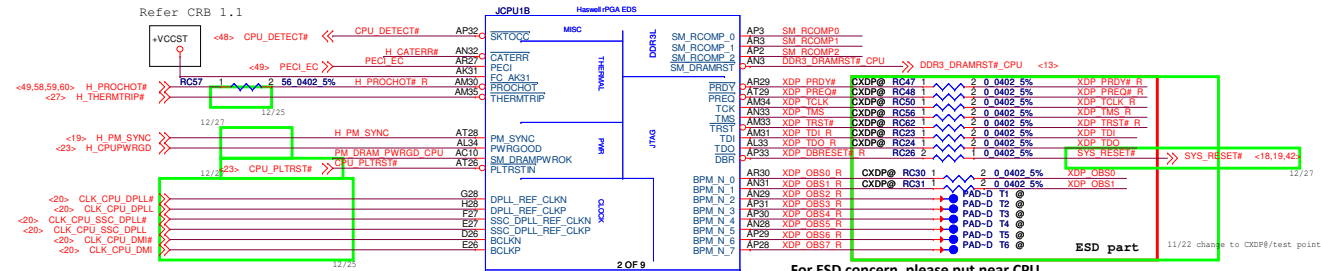
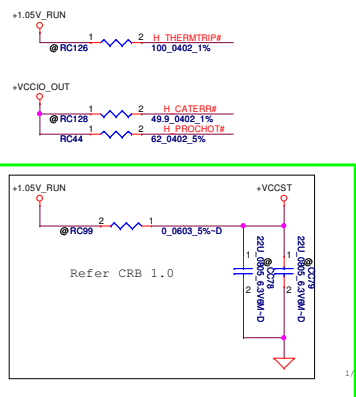
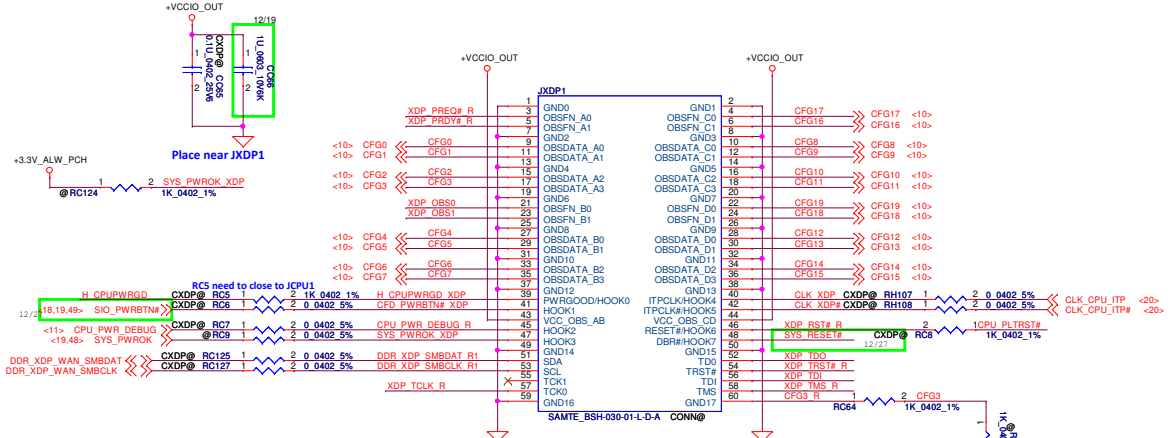
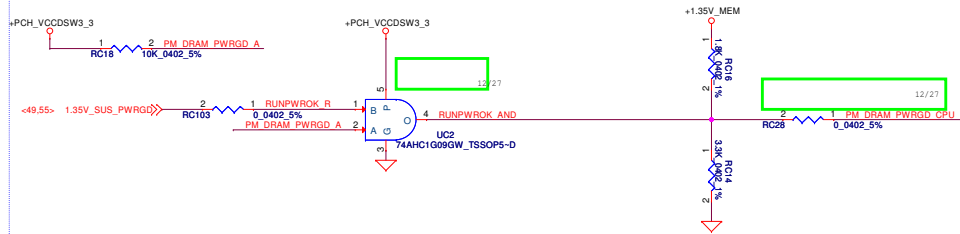
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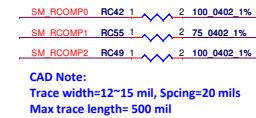
SM_DRAMPWROK with DDR Power Gating Topology



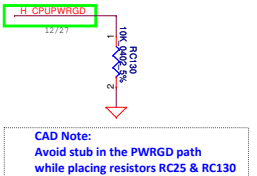
CONNG
CPU socket Reverse type.

For ESD concern, please put near CPU

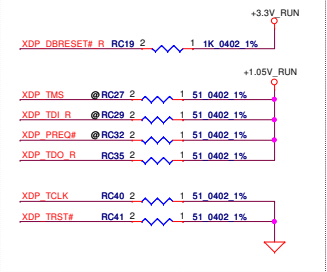
DDR3 COMPENSATION SIGNALS



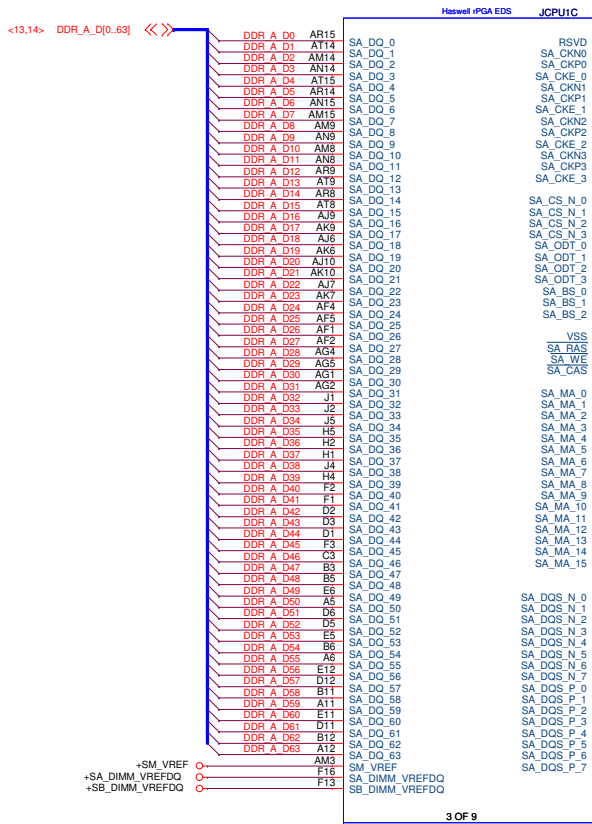
Buffered reset to CPU



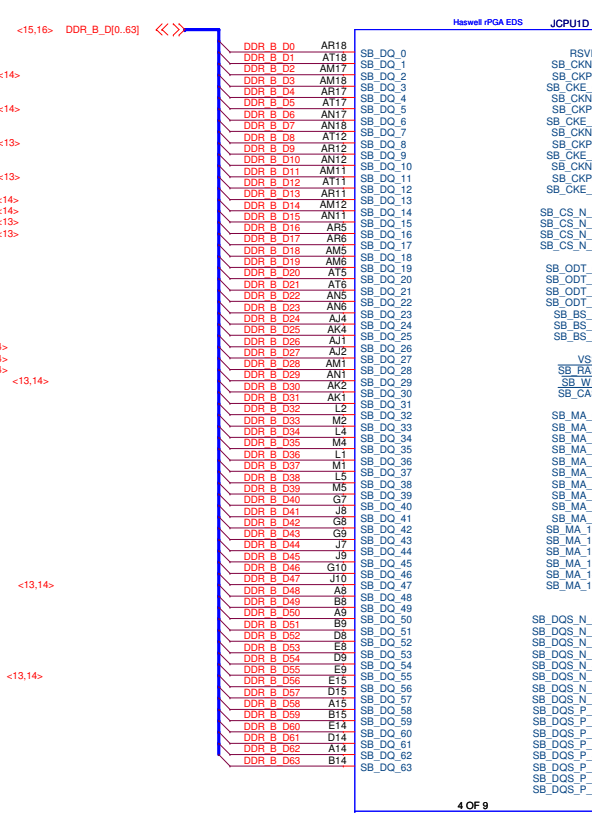
PU/PD for JTAG signals



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CONN@
CPU socket Reverse type.



CONN@
CPU socket Reverse type.

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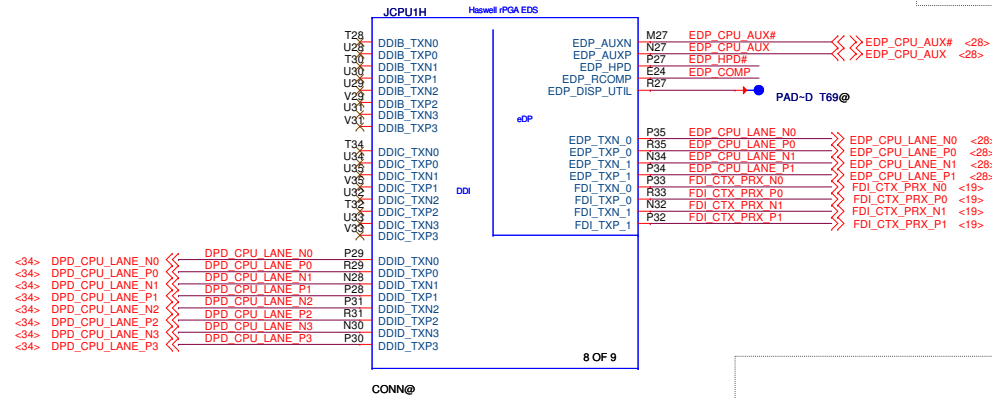
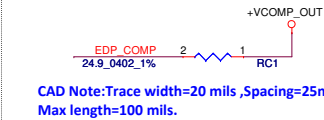
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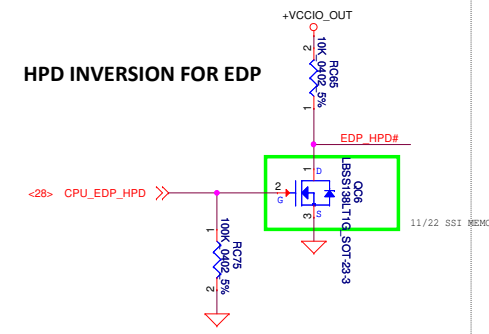


COMPENSATION PU FOR eDP



CPU socket Reverse type.

HPD INVERSION FOR EDP



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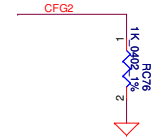
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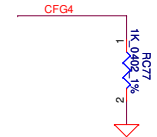
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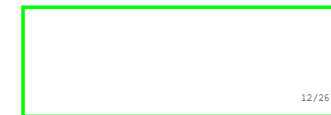
CFG STRAPS for CPU



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



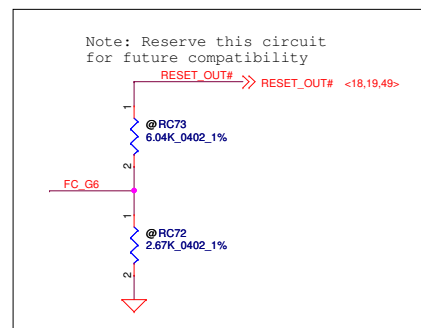
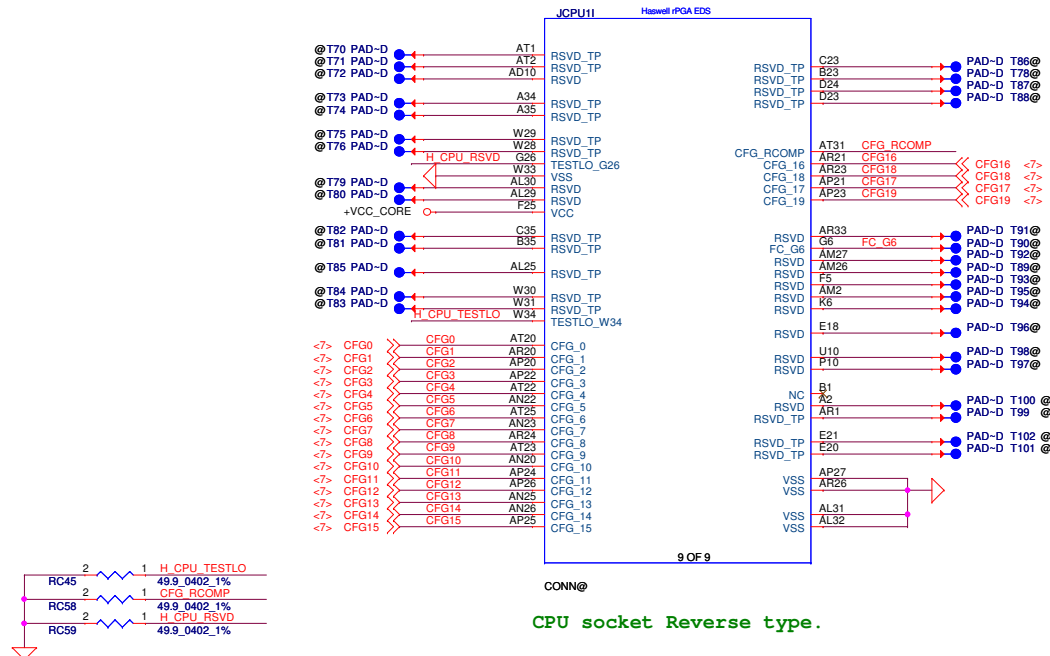
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>




PCIE Port Bifurcation Straps(PEG)	
CFG[6:5]	<p>11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8, x4, x4 - Device 1 functions 1 and 2 enabled</p>



PEG DEFER TRAINING	
CFG7	<p>1: (Default) PEG Train immediately following xRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>

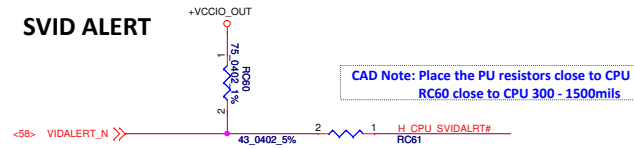


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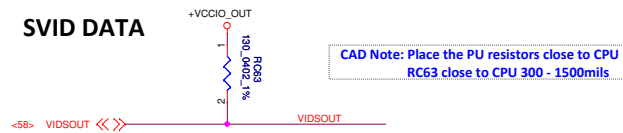
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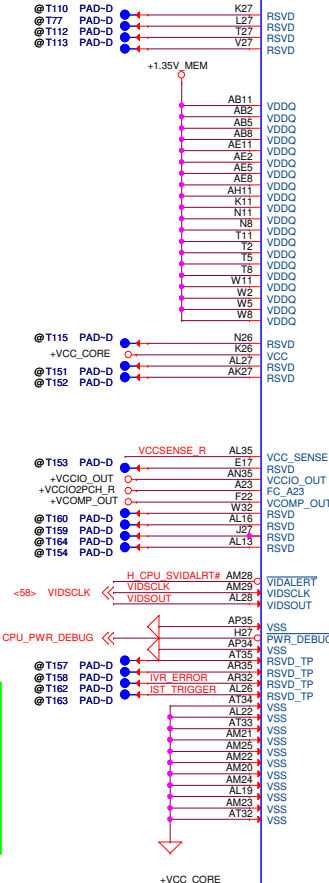
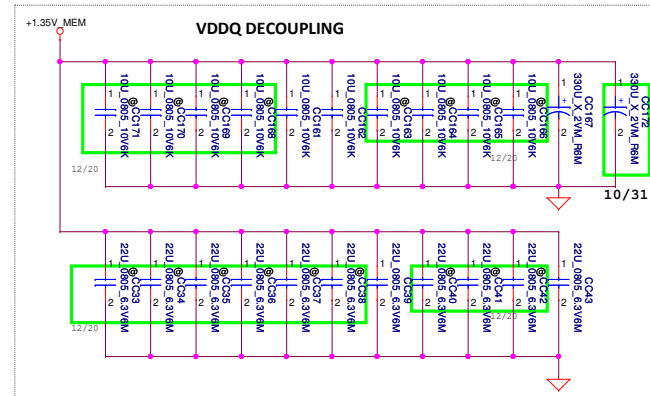
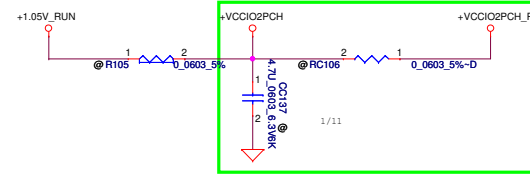
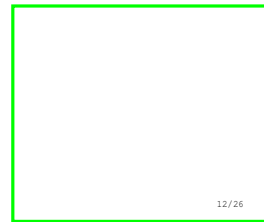
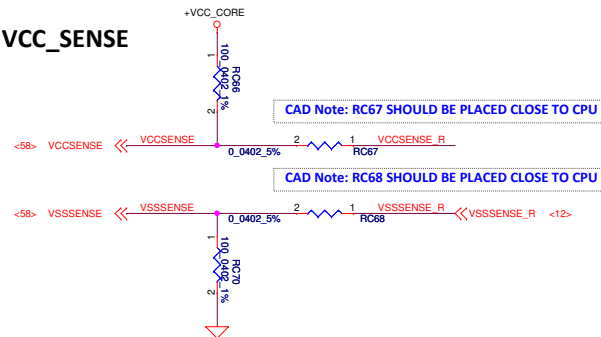
SVID ALERT



SVID DATA



VCC_SENSE



CPU socket Reverse type.

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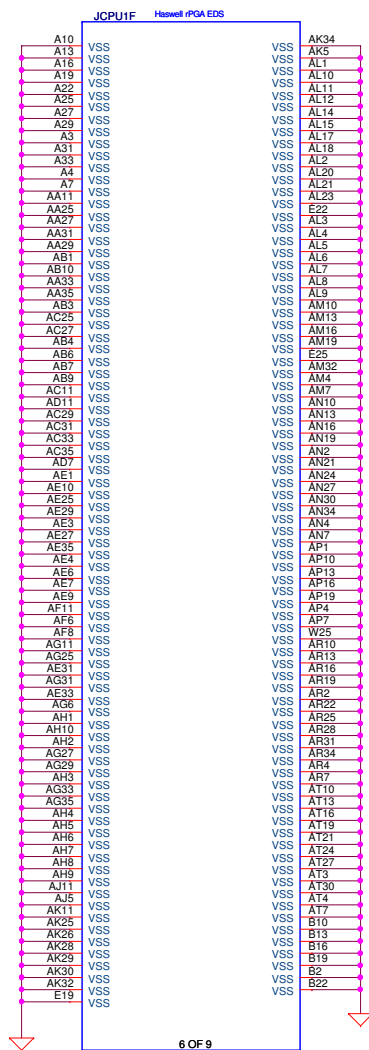


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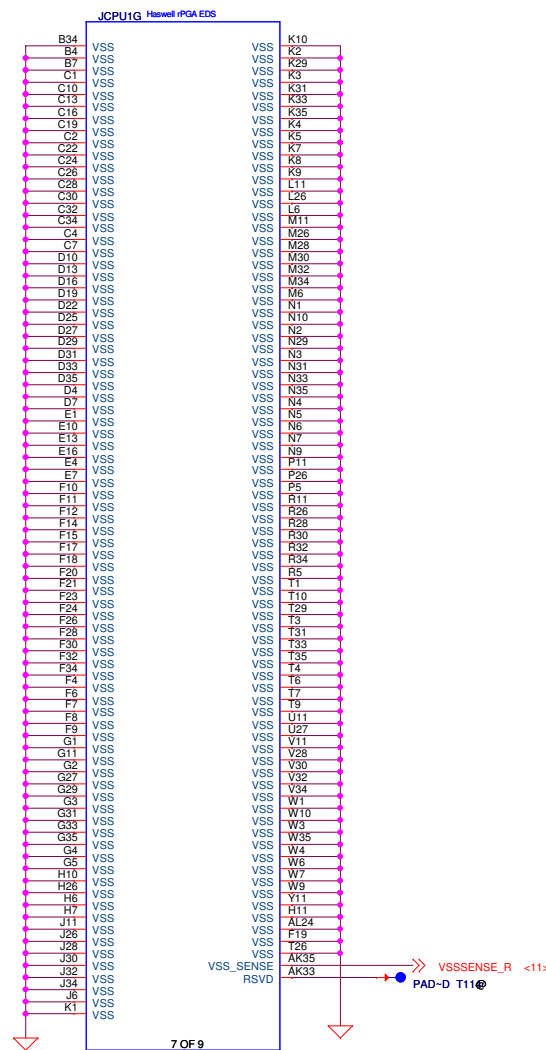
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CONN@
CPU socket Reverse type.



CONN@
CPU socket Reverse type.

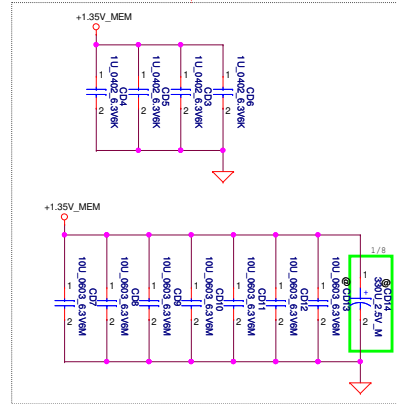
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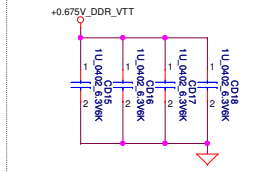
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 <14.8> DDR_A_D[0..63] <<>>
 <14.8> DDR_A_DQS[0..7] <<>>
 <14.8> DDR_A_MA[0..15] <<>>

Layout Note:
Place near JDIMM1

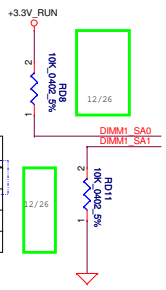


Layout Note:
Place near JDIMM1.203,204

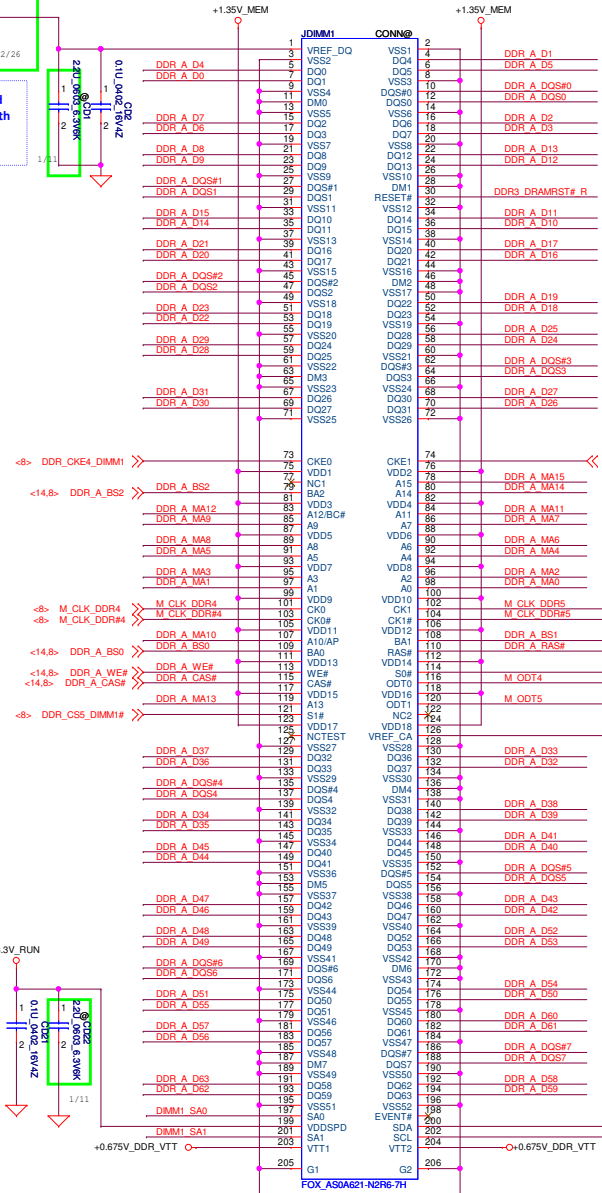


DIMM Select

SA0	SA1	
1	0	DIMM1
0	0	DIMM2
1	1	DIMM3
0	1	DIMM4



JDIMM1 REV Type H=5.2



CONN List 0925A

JDIMM3 (Ch B1 H=9.2 REV)

JDIMM1 (Ch A1 H=5.2 REV)

TOP

BOT

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

CPU

TOP

BOT

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

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JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

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```
<16,8> DDR_B_DQS#[0..7] <<>>
<16,8> DDR_B_D[0..63] <<>>
<16,8> DDR_B_DQS[0..7] <<>>
<16,8> DDR_B_MA[0..15] >>
```

JDIMM3 REV Type H=9.2

JDIMM3 (Ch B1 H=9.2 REV)

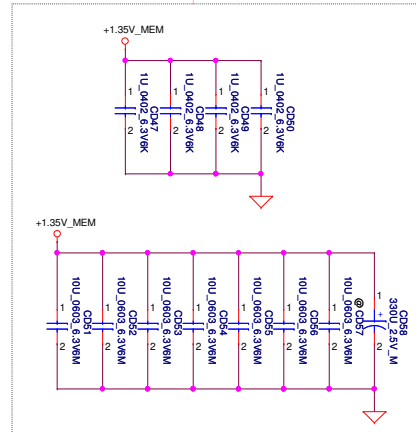
JDIMM1 (Ch A1 H=5.2 REV)

BOT

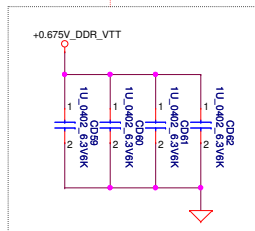
JDIMM2 (Ch A0 H=5.2 STD) JDIMM4 (Ch B0 H=5.2 REV)

Layout Note:
Place near JDIMM3

All VREF traces should have 20 mil trace width and 20 mil spacing to other signals/planes.

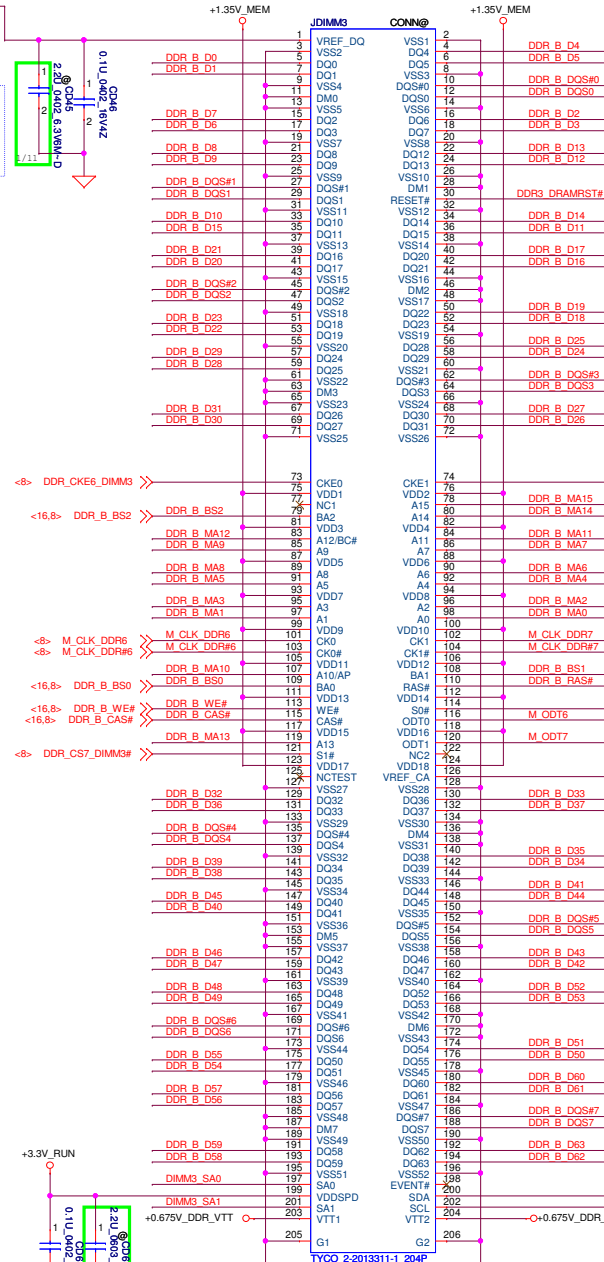
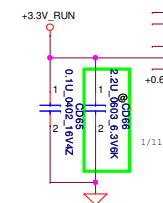
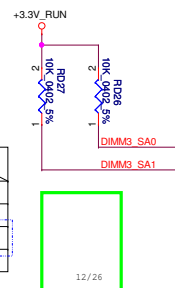


Layout Note:
Place near JDIMM3.Pin 203,204

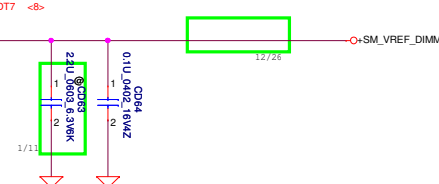
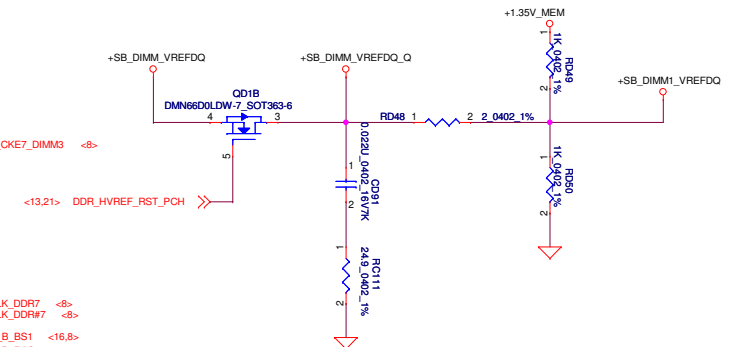


DIMM Select

SA0	SA1	
1	0	DIMM1
0	0	DIMM2
1	1	DIMM3
0	1	DIMM4



CONN List 0925A-Need update.



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JDIMM4 REV Type H=5.2

CONN List 0925A

JDIMM3 (Ch B1 H=9.2 REV)

JDIMM1 (Ch A1 H=5.2 REV)

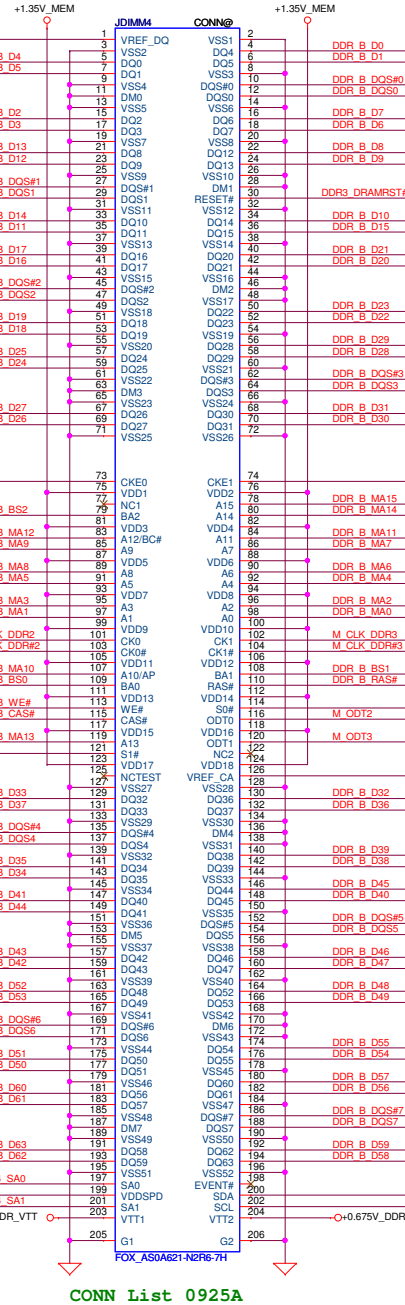
TOP

BOT

JDIMM2 (Ch A0 H=5.2 STD)

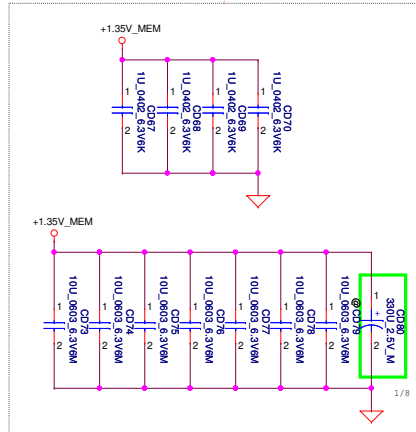
JDIMM4 (Ch B0 H=5.2 REV)

CPU

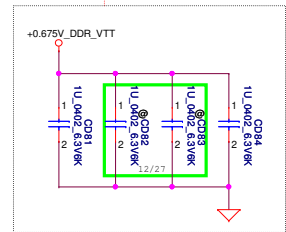


Layout Note:
Place near JDIMM4

All VREF traces should have 20 mil trace width and 20 mil spacing to other signals/planes.

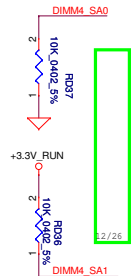


Layout Note:
Place near JDIMM4.Pin 203,204



DIMM Select

SA0	SA1	
1	0	DIMM1
0	0	DIMM2
1	1	DIMM3
0	1	DIMM4



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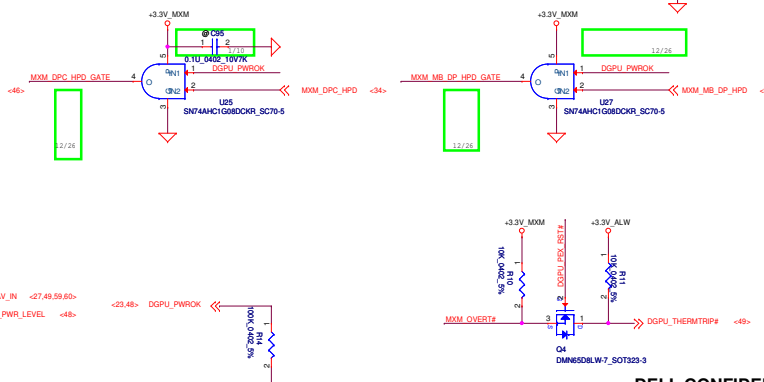
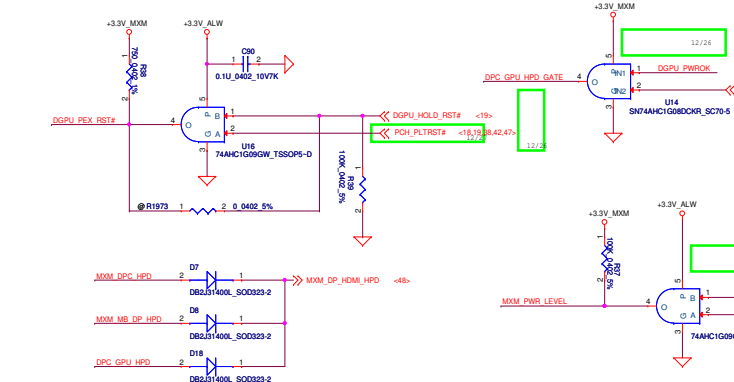
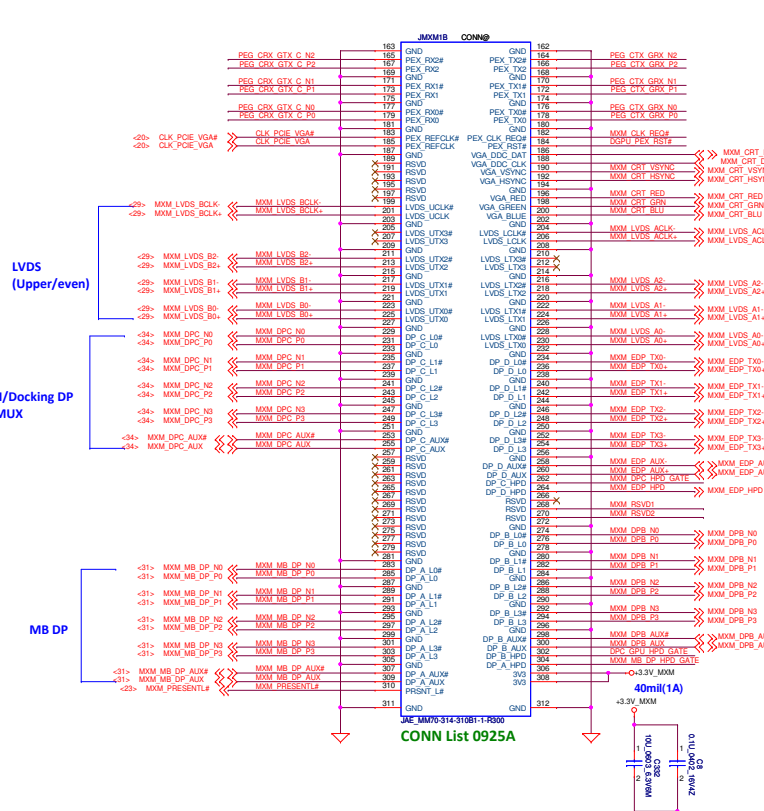
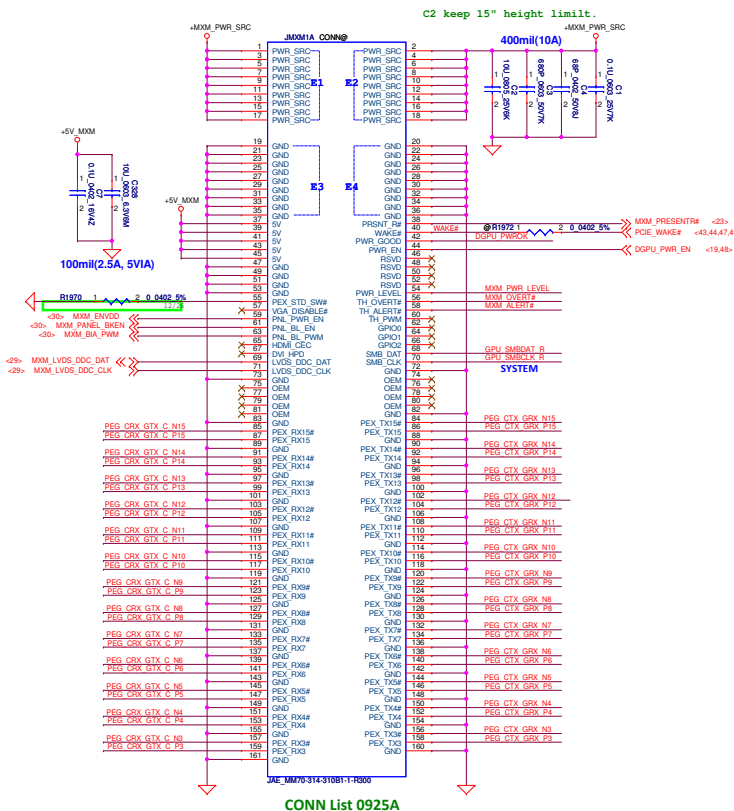
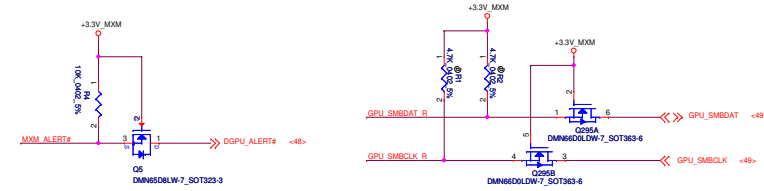
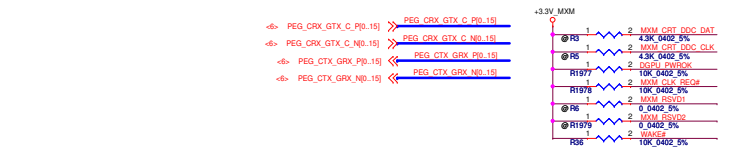
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DDRIII-SODIMM SLOT4

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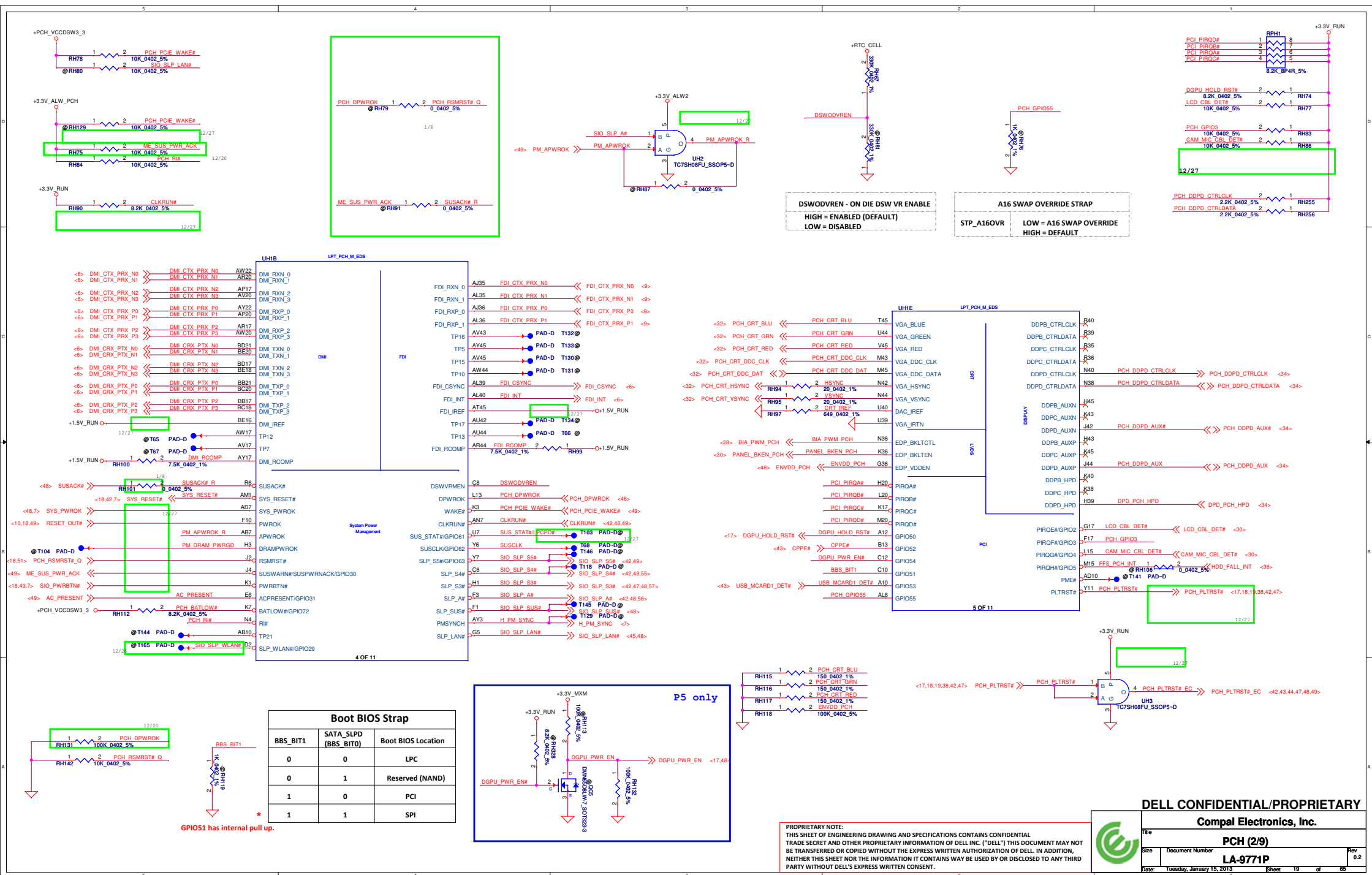


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MXM	
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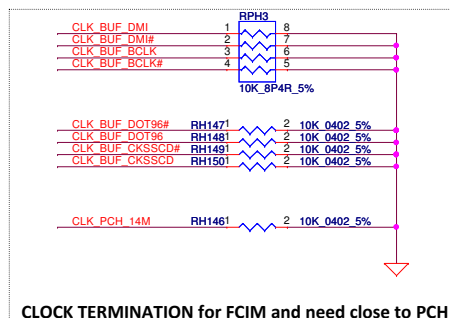
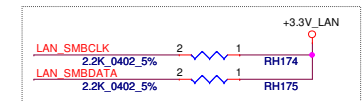
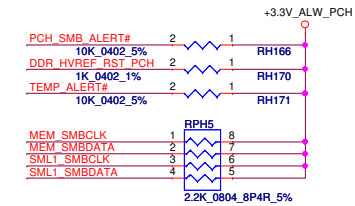
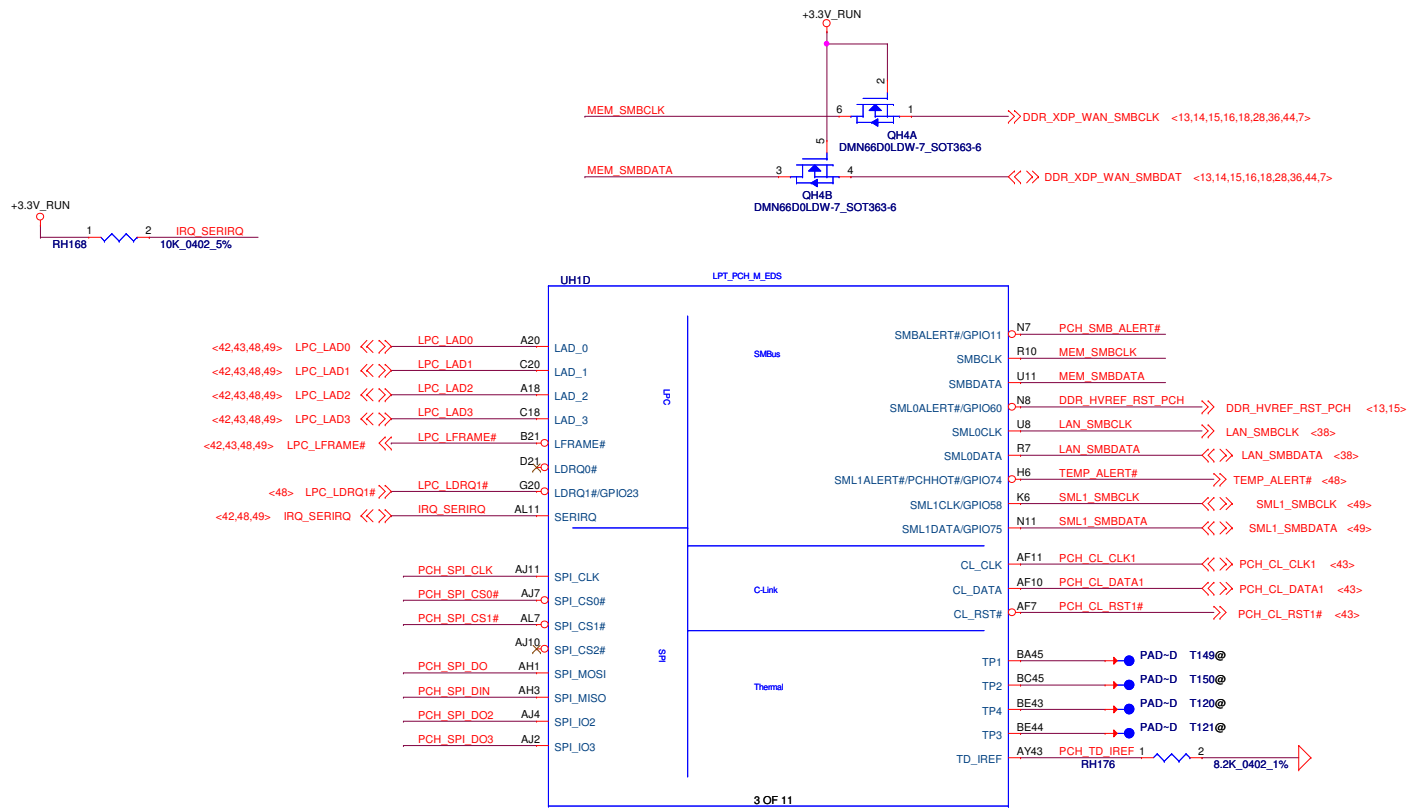


Figure 10 shows seven pinmux configurations for different clock signals. Each configuration consists of a pinmux block with two pins, 1 and 2, connected to a specific clock signal. The pinmux block is labeled with a clock signal name and a pinmux number.

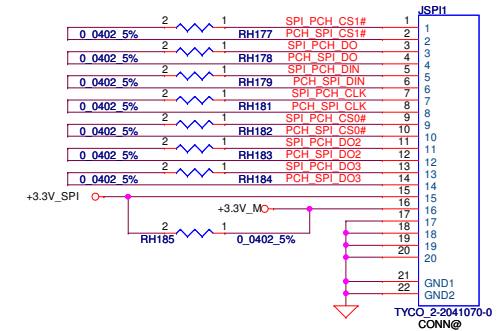
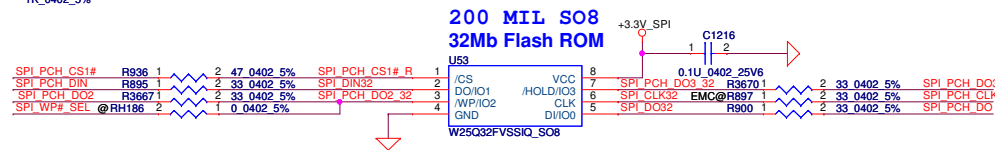
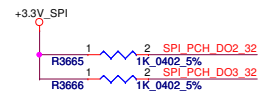
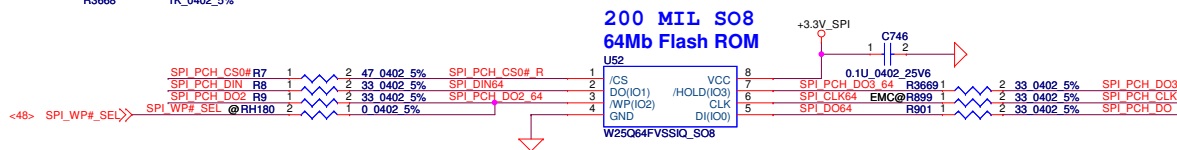
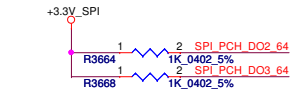
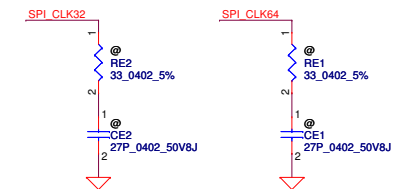
- CLK_PCI_5048**: Pinmux 0x00000000. Pin 1 is connected to CH15 (10P_0402_50M63). Pin 2 is connected to CH15 (10P_0402_50M63).
- CLK_PCI_MEC**: Pinmux 0x00000000. Pin 1 is connected to CH16 (10P_0402_50M63). Pin 2 is connected to CH16 (10P_0402_50M63).
- CLK_PCI_DOCK**: Pinmux 0x00000000. Pin 1 is connected to CH16 (10P_0402_50M63). Pin 2 is connected to CH16 (10P_0402_50M63).
- CLK_PCI_LOOPBACK**: Pinmux 0x00000000. Pin 1 is connected to CH17 (10P_0402_50M63). Pin 2 is connected to CH17 (10P_0402_50M63).
- CLK_PCI_TPM**: Pinmux 0x00000000. Pin 1 is connected to CH18 (10P_0402_50M63). Pin 2 is connected to CH18 (10P_0402_50M63).
- CLK_SIO_14M**: Pinmux 0x00000000. Pin 1 is connected to CH19 (10P_0402_50M63). Pin 2 is connected to CH19 (10P_0402_50M63).
- JETWAY_CLK14M**: Pinmux 0x00000000. Pin 1 is connected to CH180 (10P_0402_50M63). Pin 2 is connected to CH180 (10P_0402_50M63).

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if support 1MHz,need change to 499ohm+/-5%

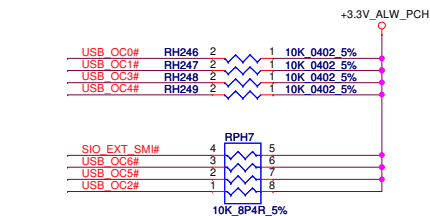
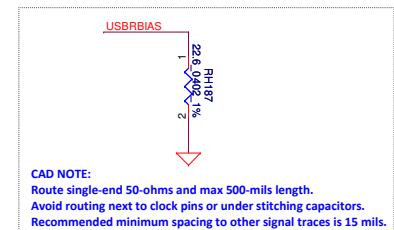
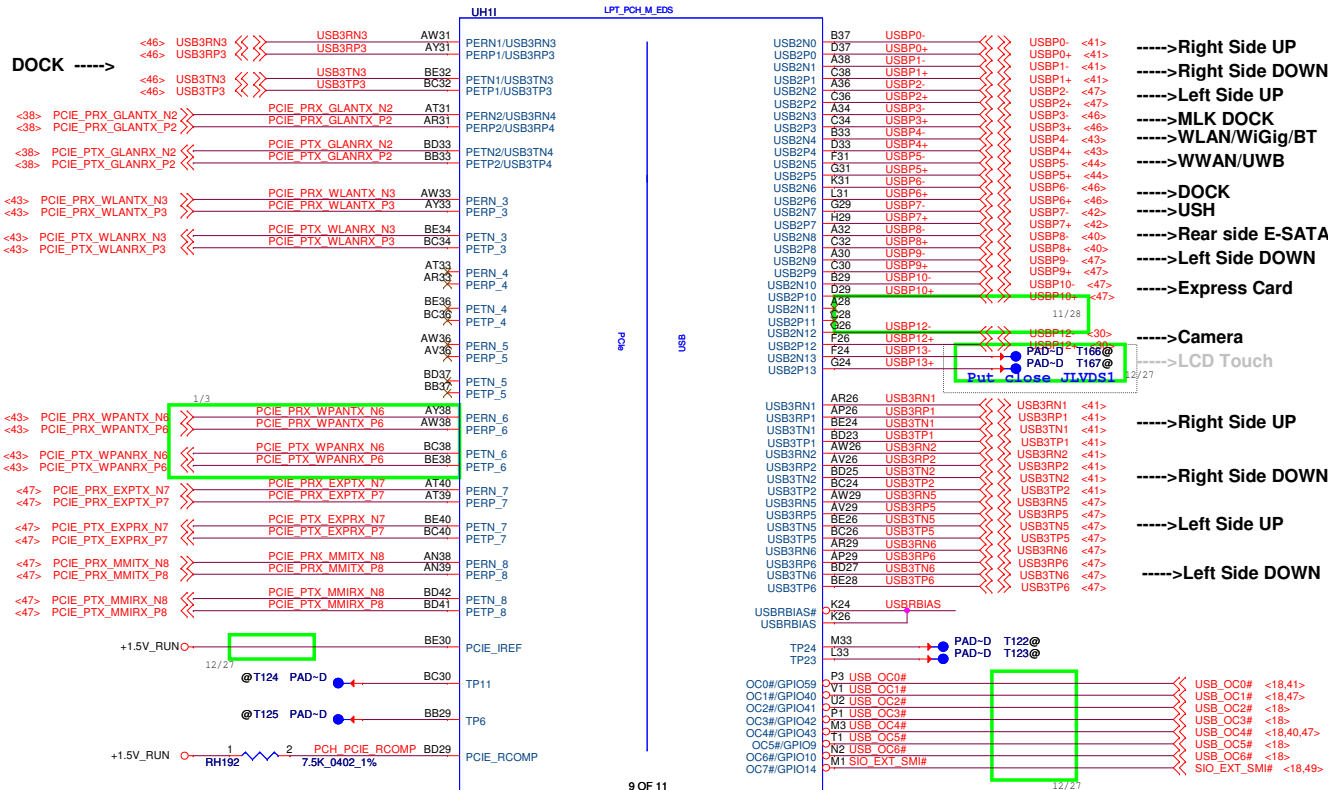


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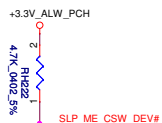
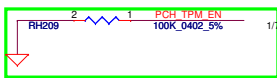
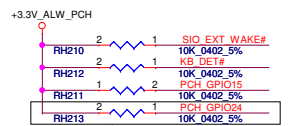
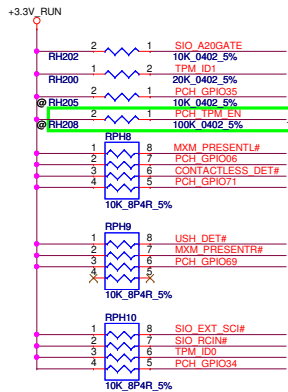
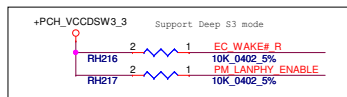
Fixed Signals				Muxed Signals				Fixed Signals				Muxed Signals				Fixed Signals			
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				(00)	(00)							(00)	(00)						
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				(01)	(01)							(01)	(01)						



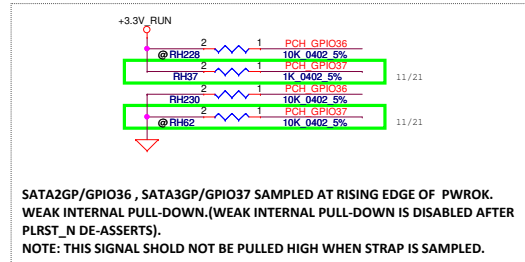
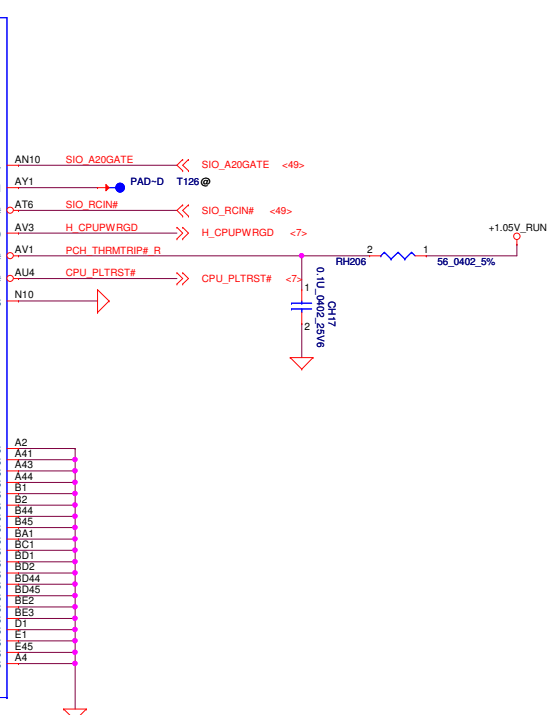
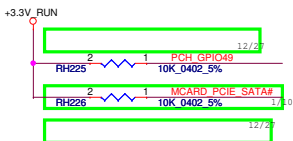
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PLL ON DIE VR ENABLE
ENABLED - HIGH(DEFAULT)
DISABLED - LOW



Note: GPIO strap option is only available for SATA/PCIE muxed signals to support mSATA/mini PCIE port switching

GPIO16	GPIO49
0: PCIE1	0: PCIE2
1: SATA4	1: SATA5

00b or 01b: Assign muxed signal to desired port
10b: Reserved
11b: Assign desired port based on GPIO

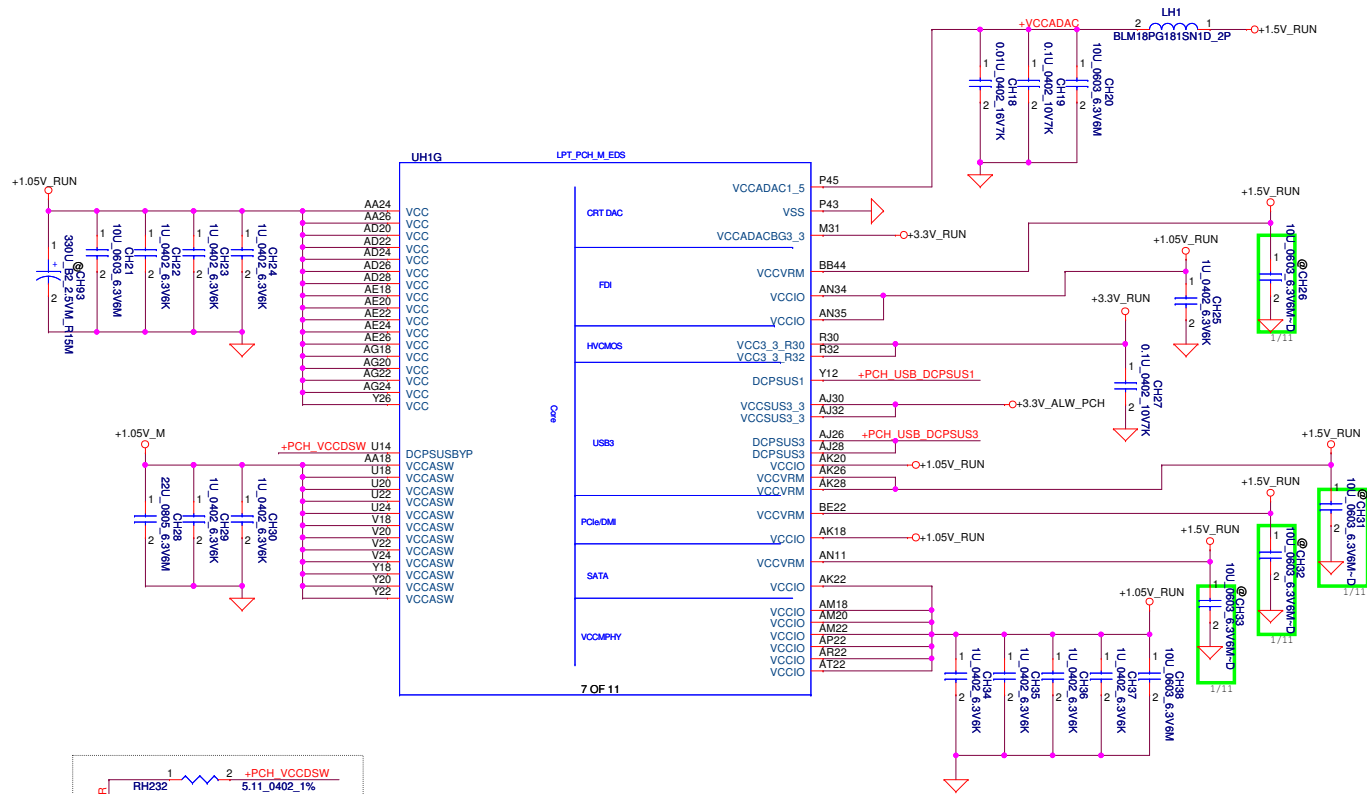
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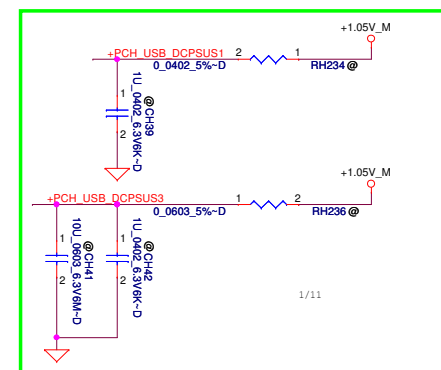
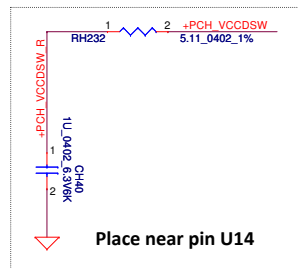
Compal Electronics, Inc.



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PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.070 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



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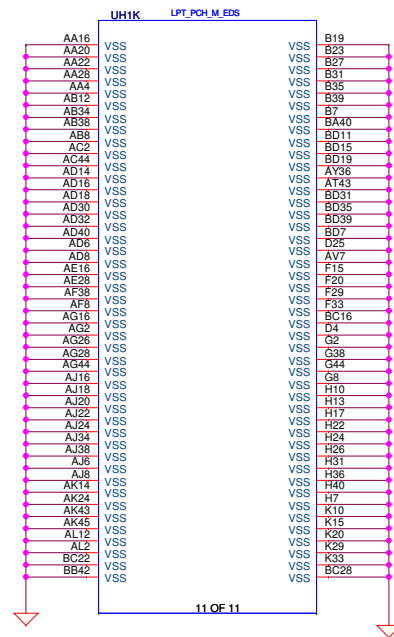
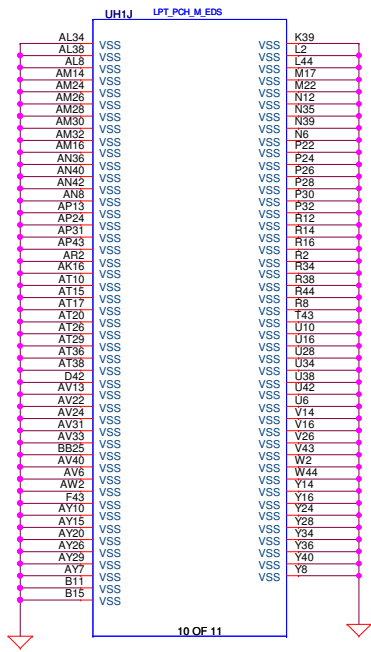
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Title: **PCH (7/9)**

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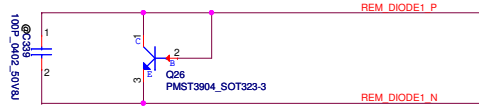


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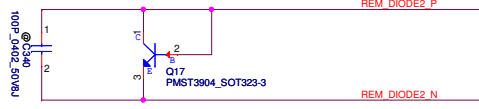


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Title			
PCH (9/9)			
Size	Document Number		Rev
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Place Q26 under CPU
Place C339 close to the Q26



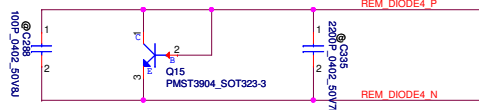
DP2/DN2 for SODIMM on Q17(TOP),
place Q17 close to SODIMM and C340 close to Q2



DP3/DN3 for Butterfly CHA on Q14(BOT),
place Q14 close to Butterfly CHA and C272 close to Q14



DP4/DN4 for Skin on Q15,
place Q15 close to Vcore VR choke and C288 close to Q15

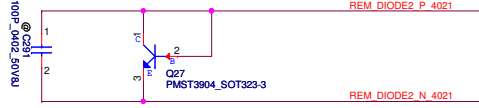


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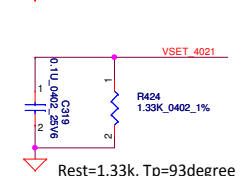
Place Q16 under MXM(TOP side)
Place C273 close to the Q16



DP2/DN2 for MXM on Q27(BOT side),
place Q27 close to Butterfly CHB and C291 close to Q27

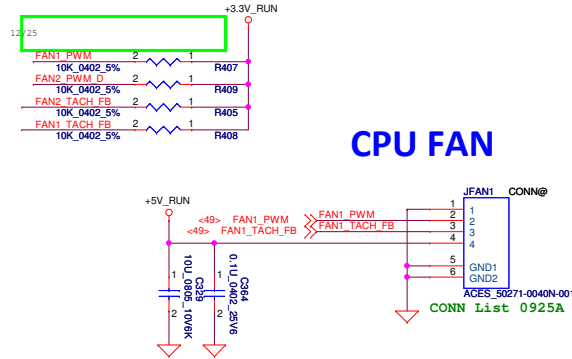


R430 10K_0402_5%
VCP_4021

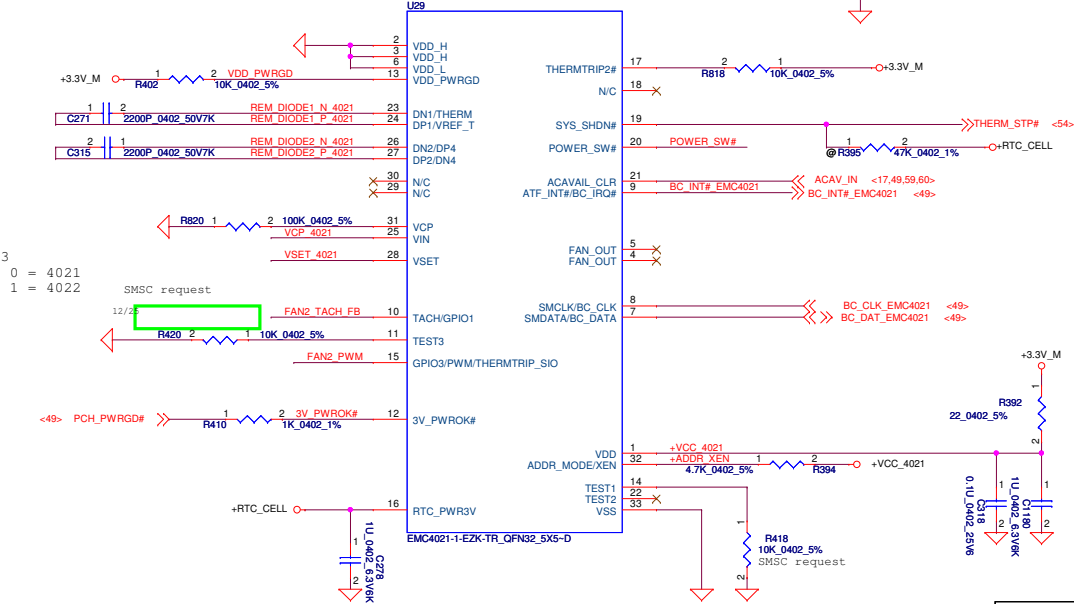
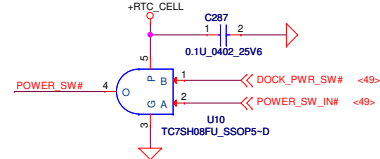
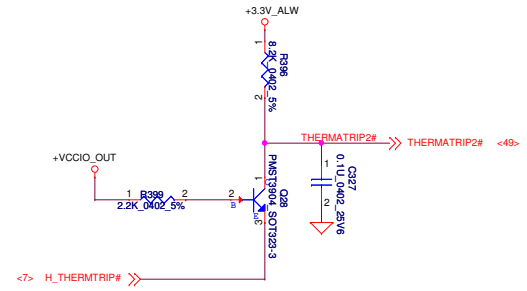
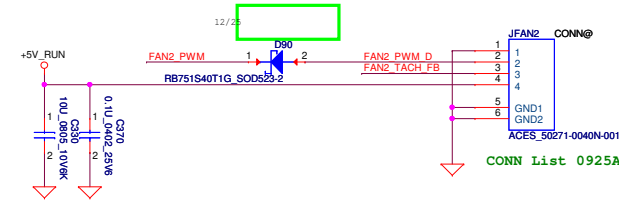


Rest=1.33k, Tp=93degree

CPU FAN



MXM FAN



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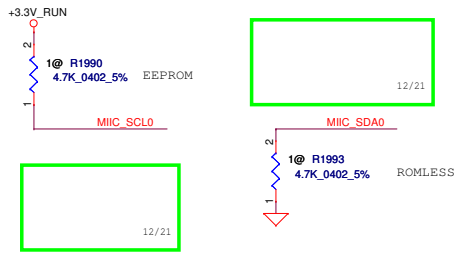
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FAN control

LA-9771P

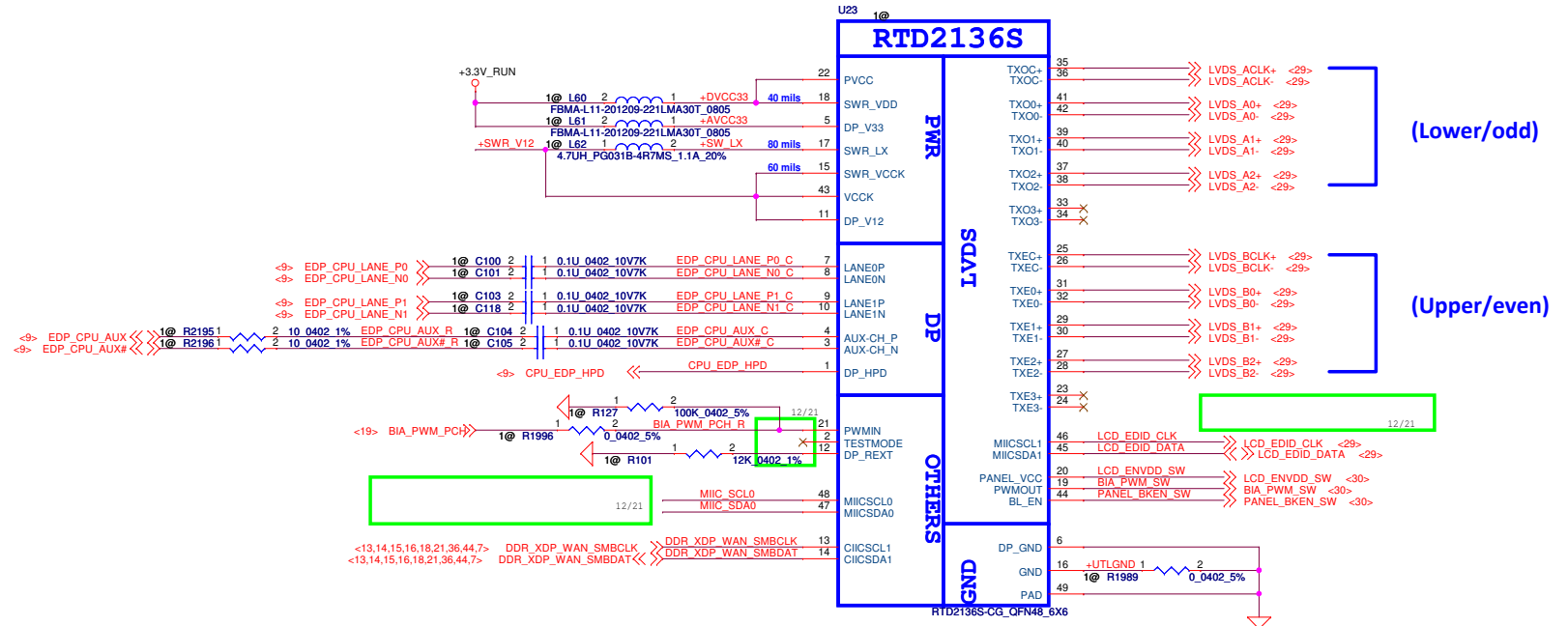
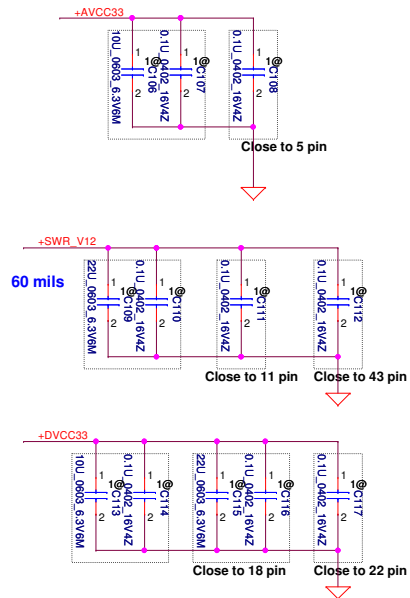
Date: Tuesday, January 15, 2013 Sheet 27 of 65

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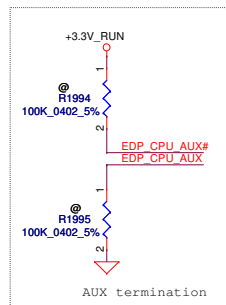
Power Consumption:

- Pin5 (DPV33) < 20mA
- Pin 11 (DPV12) < 100mA
- Pin 15 (SWR_VCKK) < 100mA (layout trace > 60 mil)
- Pin 17 (SWR_LX) < 600mA (layout trace > 80 mil for LDO mode)
- Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
- Pin 22 (PVCC) < 50 mA
- Pin 43 (VCKK) < 50mA



1009 change to SA000067100 (RTD2136R)

* RTD2136R SA000067100 : Populate R1993



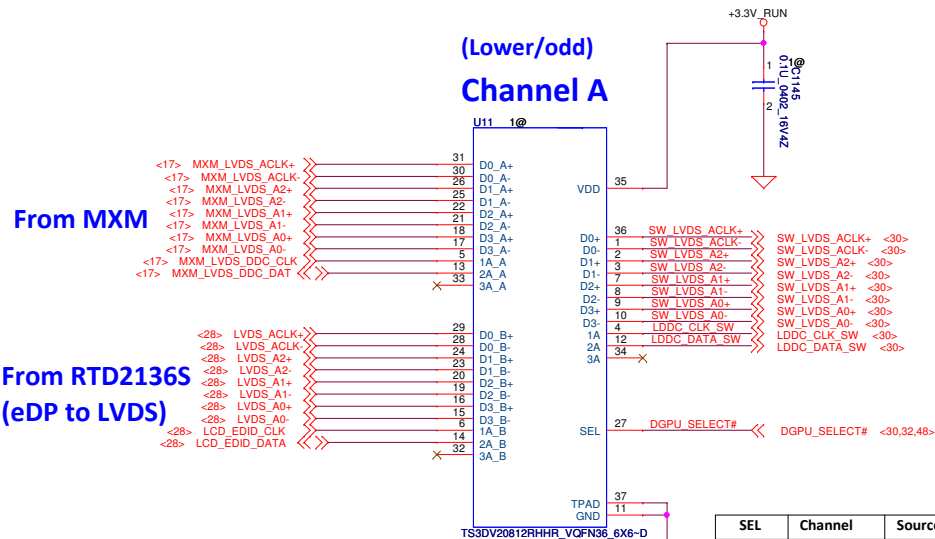
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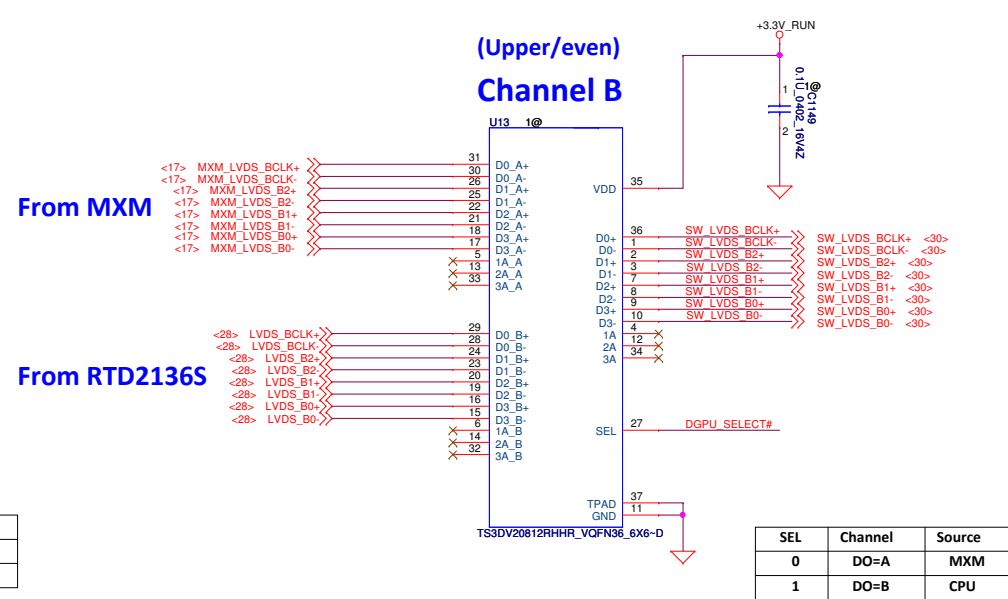
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Size	Document Number	LA-9771P	
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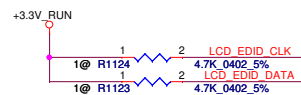


SEL	Channel	Source
0	DO=A	MXM
1	DO=B	CPU



SEL	Channel	Source
0	DO=A	MXM
1	DO=B	CPU

12/25
if phase in 2nd GFX Card, must check DDC_CLK/DATA has pulled up on GFX card.

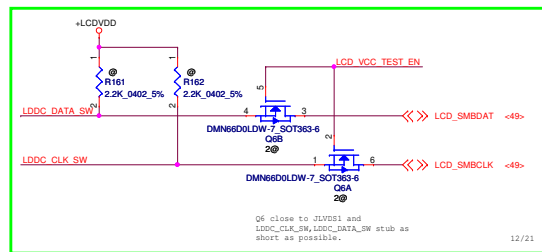
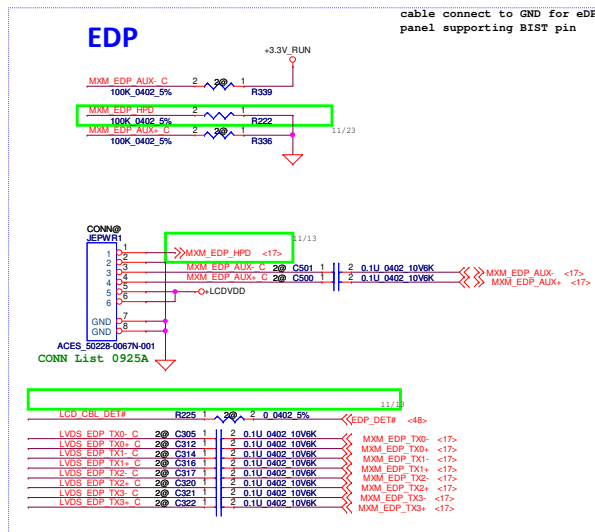
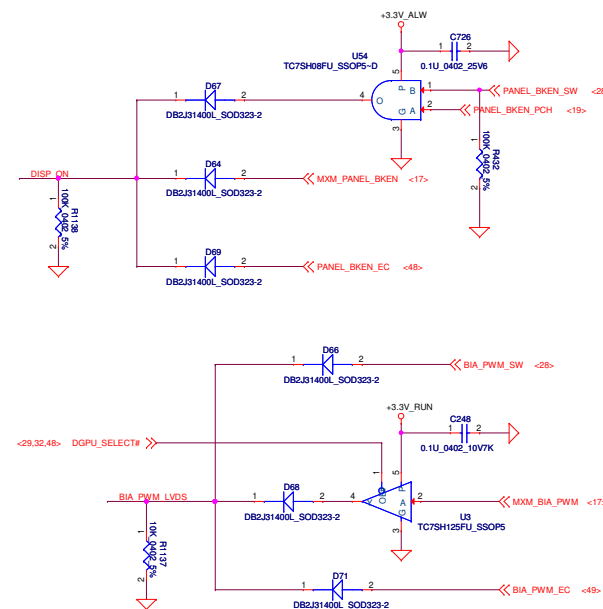
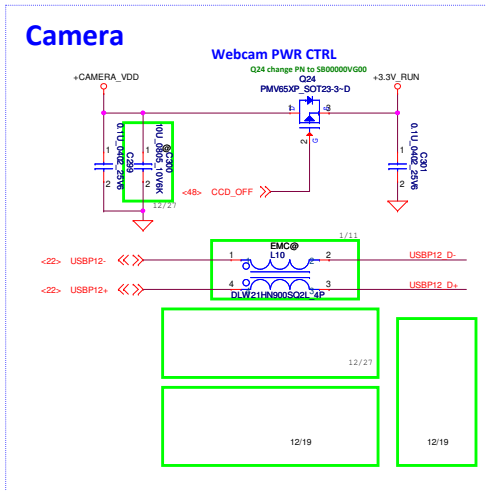
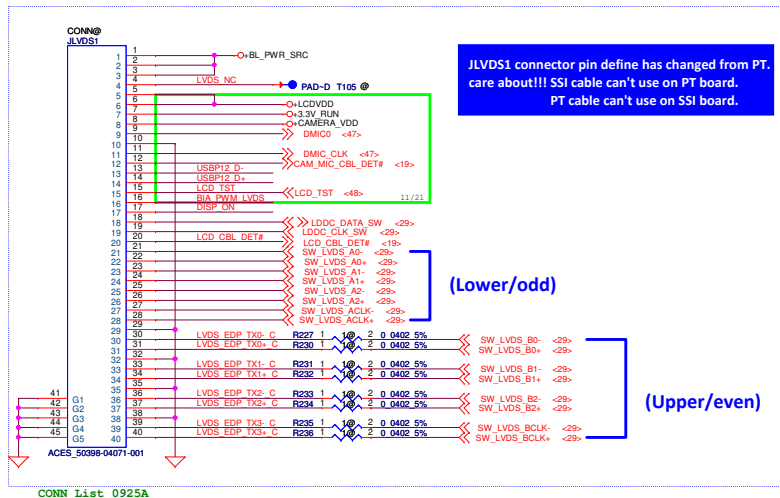
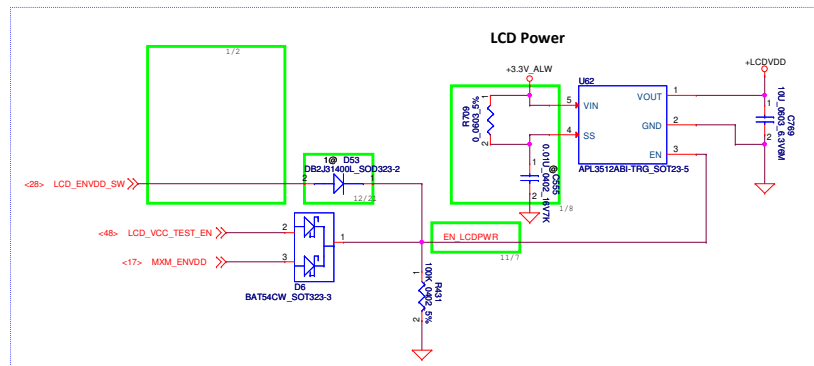
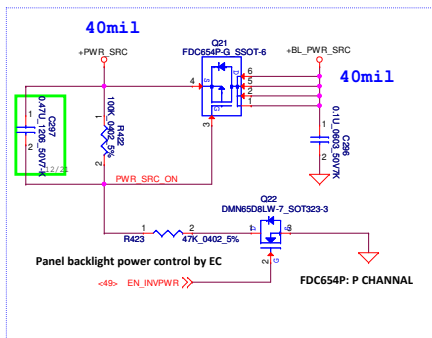
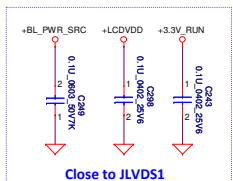
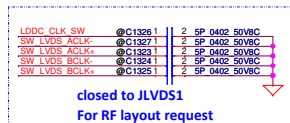
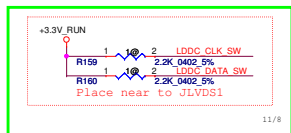


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Title LVDS SW		
Size	Document Number LA-9771P	Rev 0.2
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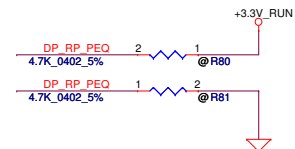
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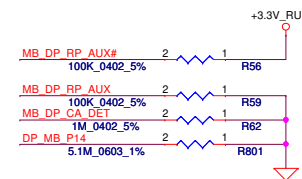
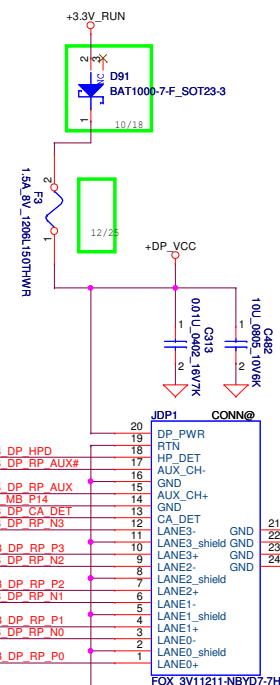


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Programmable input equalization levels; Internal pull down at ~150k Ω , 3.3V I/O.
 L: default, LEQ, compensate channel loss up to 12dB @ HBR2
 H: HEQ, compensate channel loss up to 15dB @ HBR2
 M: LLEQ, compensate channel loss up to 5dB @ HBR2



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DP Conn

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For debug issue that (DF543750)DP->HDMI/DP->S-DVI dongle
no function on NV units
Add TMDS DDC pull up schematic on DP port

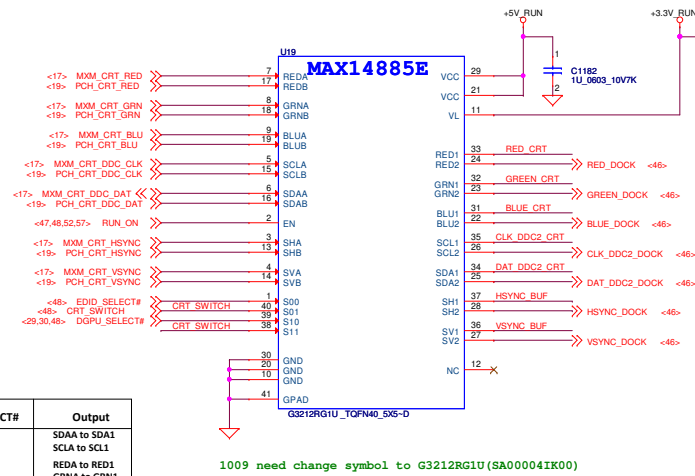
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Channel A --> MXM

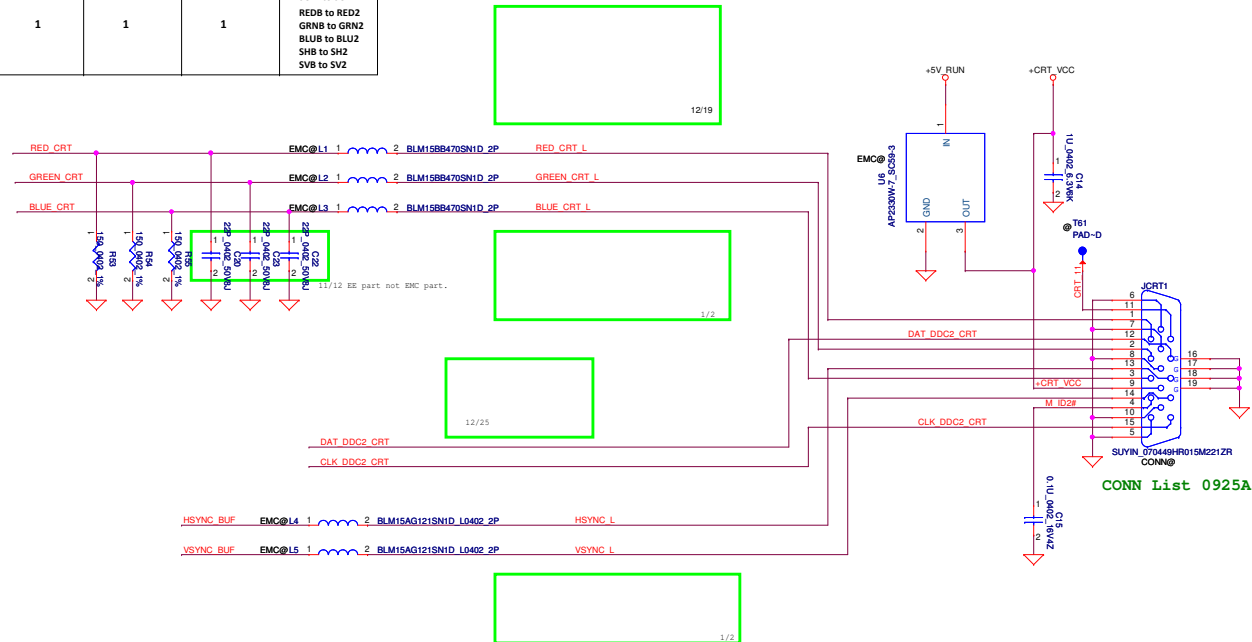
Channel B --> PCH

	CRT_SWITCH	DGPU_SELECT#	EDID_SELECT#	Output
DSC mode output to MB VGA	0	0	0	SDAA to SDA1 SCLA to SCL1 REDA to RED1 GRNA to GRN1 BLUA to BLU1 SHA to SH1 SVA to SV1
DSC mode output to docking VGA	1	0	0	SDAA to SDA2 SCLA to SCL2 REDA to RED2 GRNA to GRN2 BLUA to BLU2 SHA to SH2 SVA to SV2
UMA mode output to MB VGA	0	1	1	SDAB to SDA1 SCLB to SCL1 REDB to RED1 GRNB to GRN1 BLUB to BLU1 SHB to SH1 SVB to SV1
UMA mode output to docking VGA	1	1	1	SDAB to SDA2 SCLB to SCL2 REDB to RED2 GRNB to GRN2 BLUB to BLU2 SHB to SH2 SVB to SV2



Port 1 --> MB board CRT

Port 2 --> Docking Port RGB



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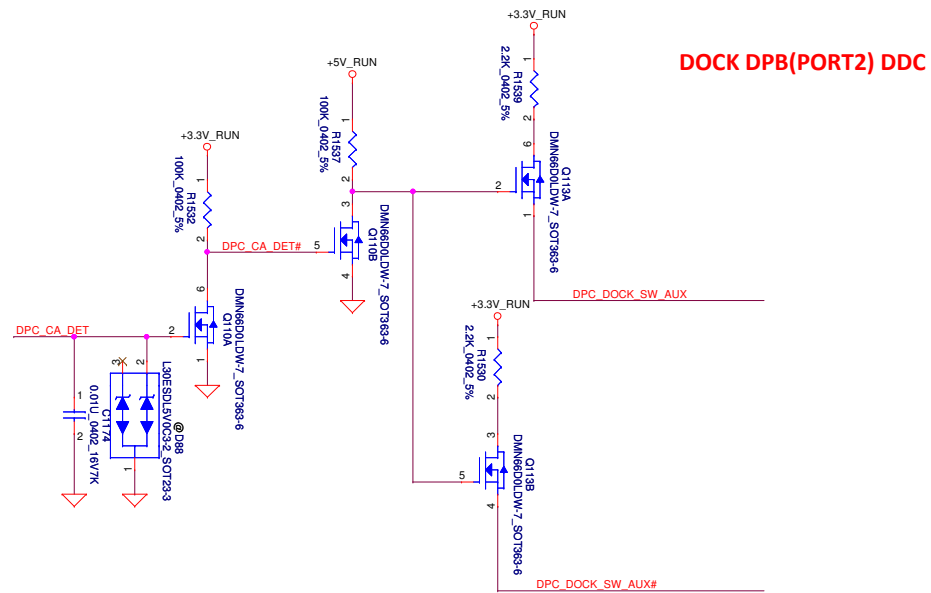
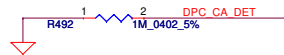
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Size	Document Number	LA-9771P	
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[illegible]

	CA_DET	Output
HDMI/DVI	1	A2=B2 A3=B3
DP	0	A0=B0 A1=B1



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Title			
DP DDC SW			
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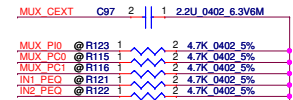
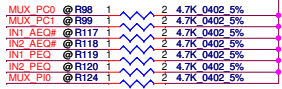
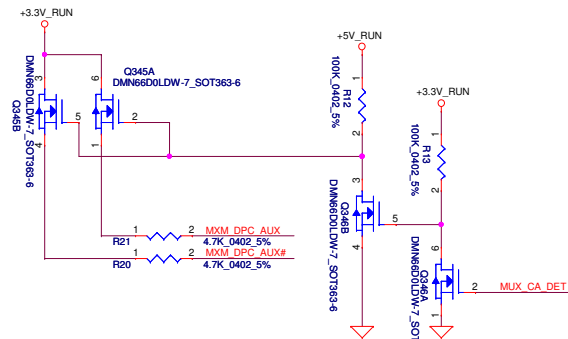
From MXM

From CPU

CIS LINK OK

To DEMUX

DOCK DPA(PORT1) DDC & HDMI DDC-before PS8331



SW	Channel	Source
0(default)	DO=IN1	MXM
1	DO=IN2	CPU

INy_PEQ(y=1,2)
L:default,LEQ, compensate channel loss up to 11.5dB @HBR2
H:HEQ,compensate channel loss up to 14.5dB @HBR2
M:LLEQ,compensate channel loss up to 8.5dB @HBR2

INy_AEQ(y=1,2)
L: Automatic EQ enable (default)
H: Automatic EQ disable

PI0
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PC0
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1
L: default
H: Output swing +20%
M: Output swing -16.7%

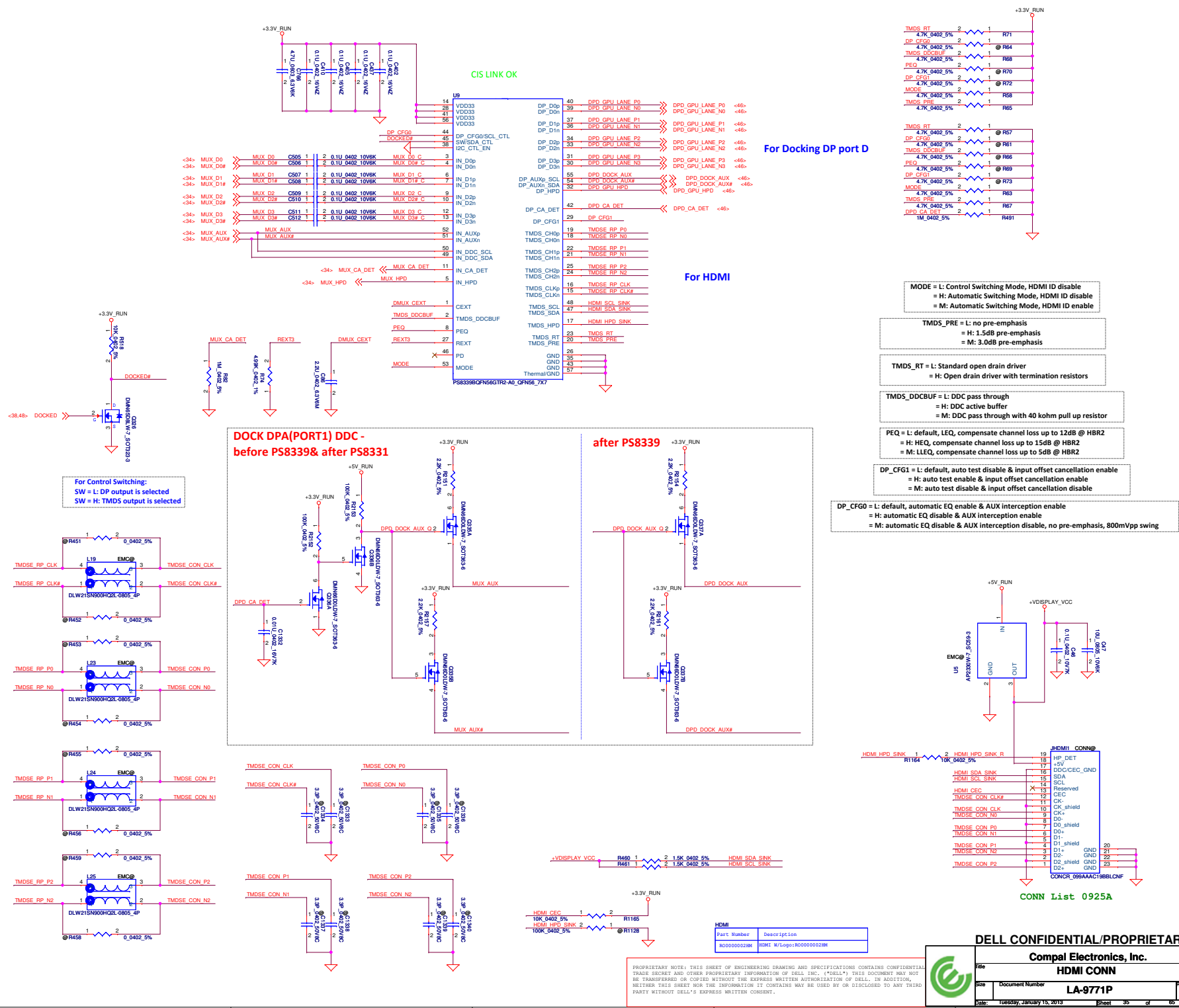
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Title		DP MUX	
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HDD PWR

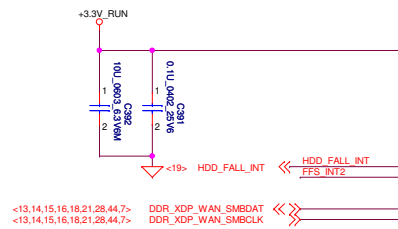
+5V_RUN +5V_HDD

2 1

PJP33

JUMP_43X79

SHORT DEFAULT

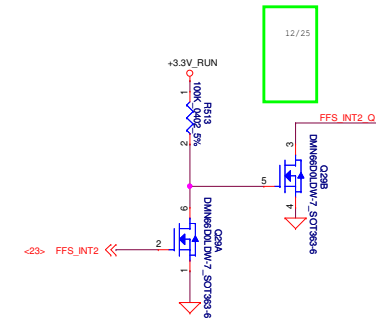


U88

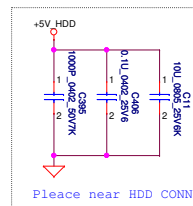
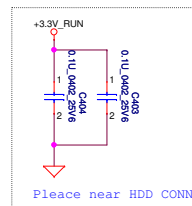
LQ63DM

1 VDD_ID RES 10
 14 VDD RES 13
 9 INT 1 RES 15
 10 INT 2 RES 16
 7 SDO/SA0 GND 5
 6 SCL / SDI / SDO GND 12
 4 SDA/SPC
 8 CS 2
 NC 3
 NC

LQ63DMTR_LGA16_3X3-D



CONN list 0925A

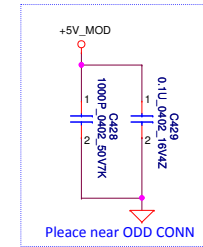
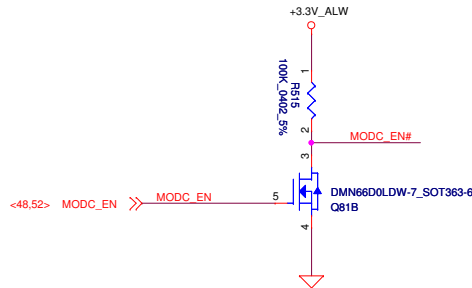
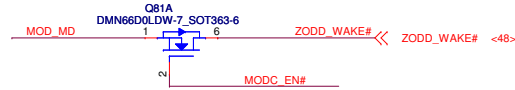
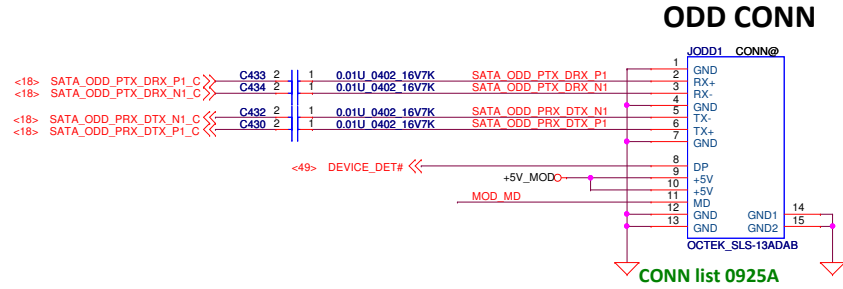
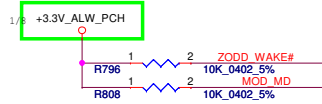


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Title	
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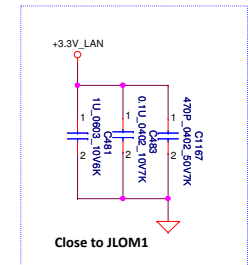
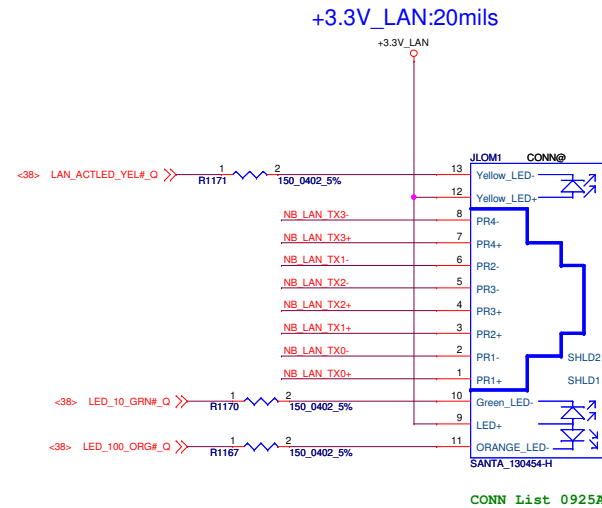
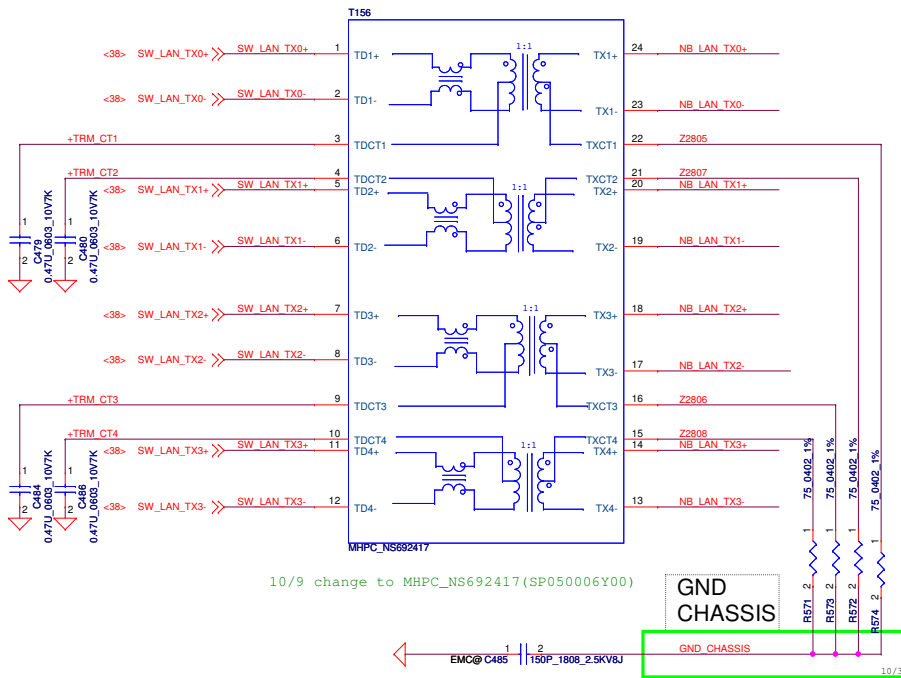
Compal Electronics, Inc.

ODD CONN

LA-9771P

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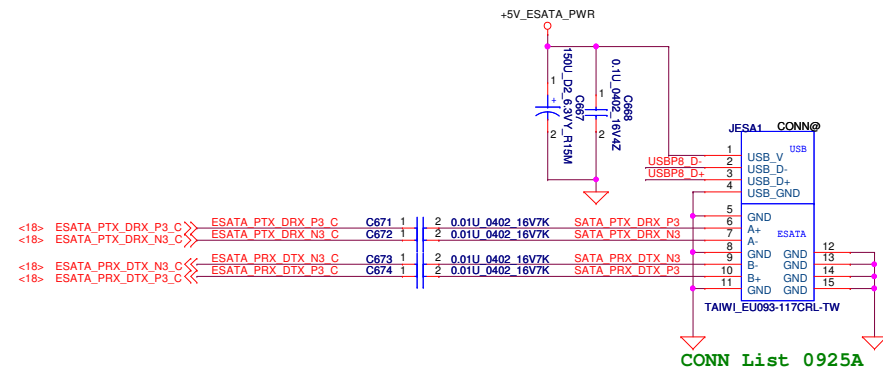
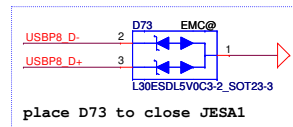
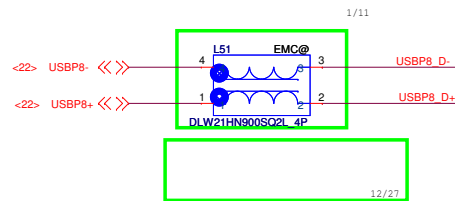
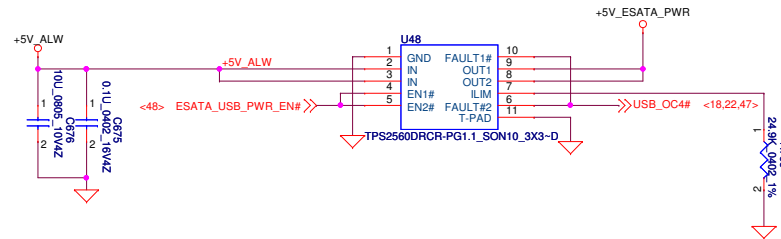


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Title			RJ45
Size	Document Number	LA-9771P	
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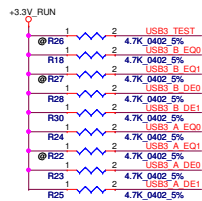
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Title			ESATA
Size	Document Number	LA-9771P	
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11/30

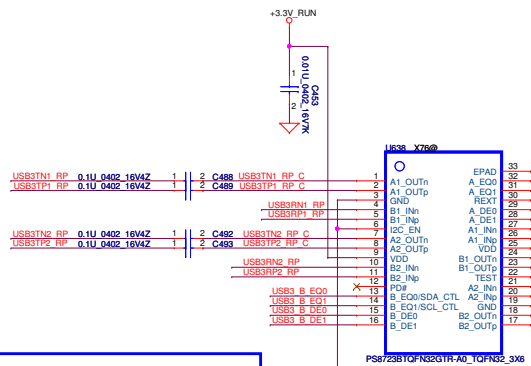
EQ : Equalizer control and program.
3.3V tolerant. Internally pulled down at ~150K ohm
[A_EQ1, A_EQ0] = [B_EQ1, B_EQ0]
LL: program EQ for channel loss up to 9.5dB
LH: program EQ for channel loss up to 13dB
HH: program EQ for channel loss up to 17dB

TEST : Chip test mode enable.
3.3V tolerant. Internally pulled down at ~150K ohm.
L: Normal operation (default)
H: Test mode enable
for compliance test, this pin should be pulled to high.

Pin 13 : B_EQ0 / SDA_CTL
Pin 14 : B_EQ1 / SCL_CTL
Pin 15 : B_DE0 / I2C_ADDR0
Pin 16 : B_DE1 / I2C_ADDR1

DE : Programmable output pre-emphasis level setting.
3.3V tolerant. Internally pulled down at ~150K ohm
[A_DE1, A_DE0] = [B_DE1, B_DE0]
LL: 5.0dB de-emphasis
LH: No de-emphasis
HL: 2.0dB de-emphasis
HH: 5.0dB de-emphasis

Pin 28 : A_DE1 / NC
Pin 29 : A_DE0 / NC
Pin 31 : A_EQ1 / NC
Pin 32 : A_EQ0 / NC

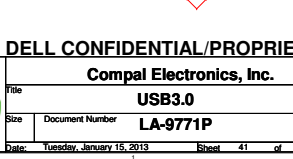
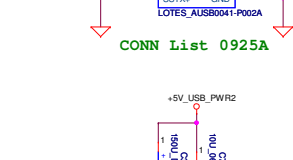
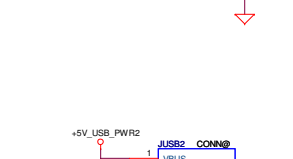
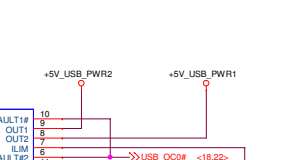
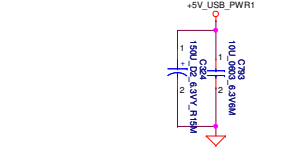
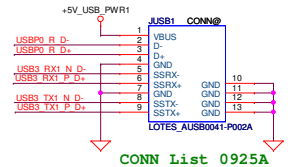
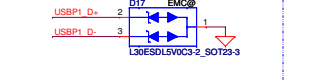
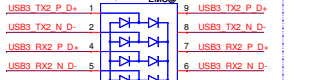
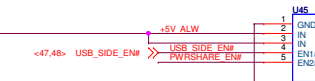
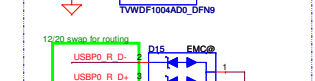
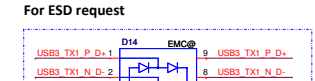
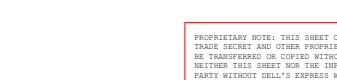
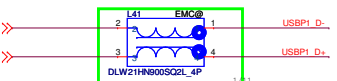
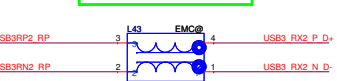
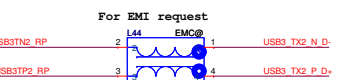
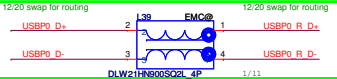
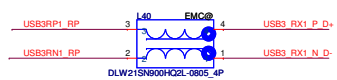
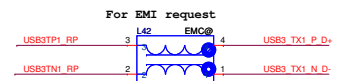


PD# : chip power down, active LOW, 3.3V tolerant,
internally pulled up at ~150K ohm.

<48> USB_PWR_SHR_VBUS_EN#

CB=0 autodetection charger identification active
CB=1 charging downstream port with active USB2.0 data communication mode with 1.5A support

CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)



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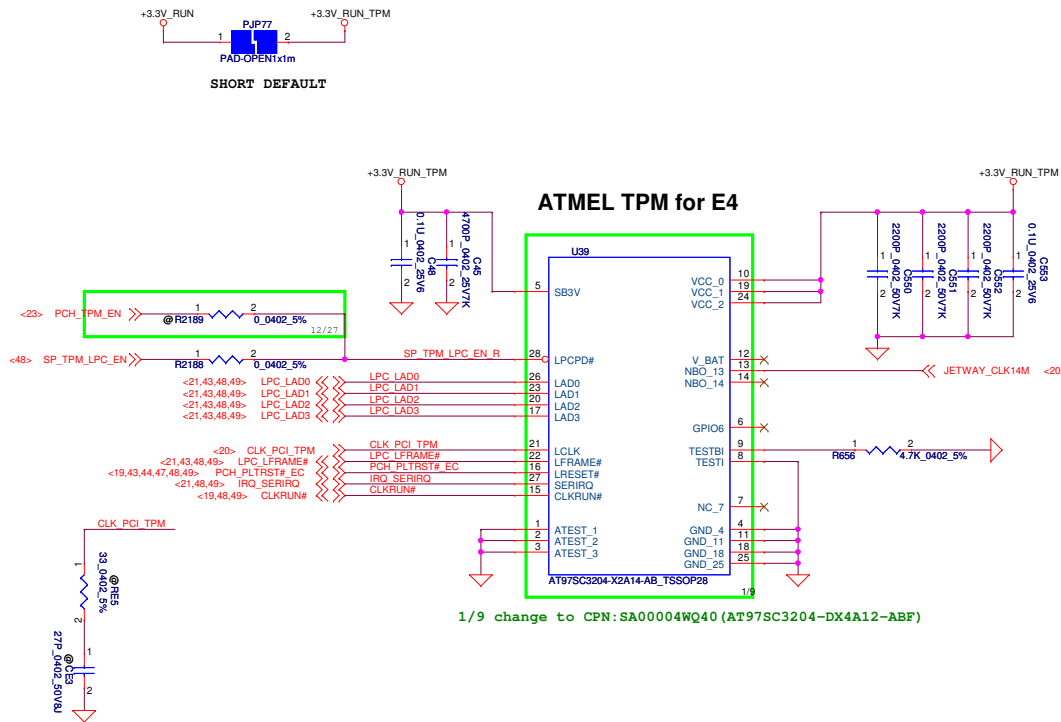
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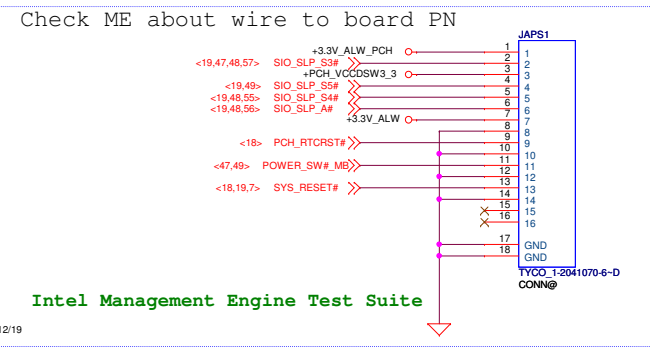
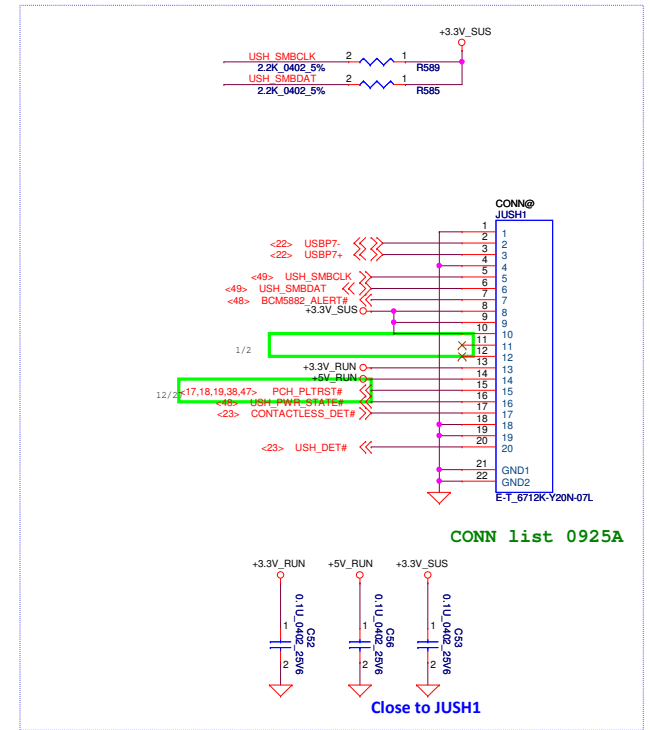
USB3.0

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Size Document Number
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1/9 change to CPN:SA00004WQ40 (AT97SC3204-DX4A12-ABF)



Intel Management Engine Test Suite

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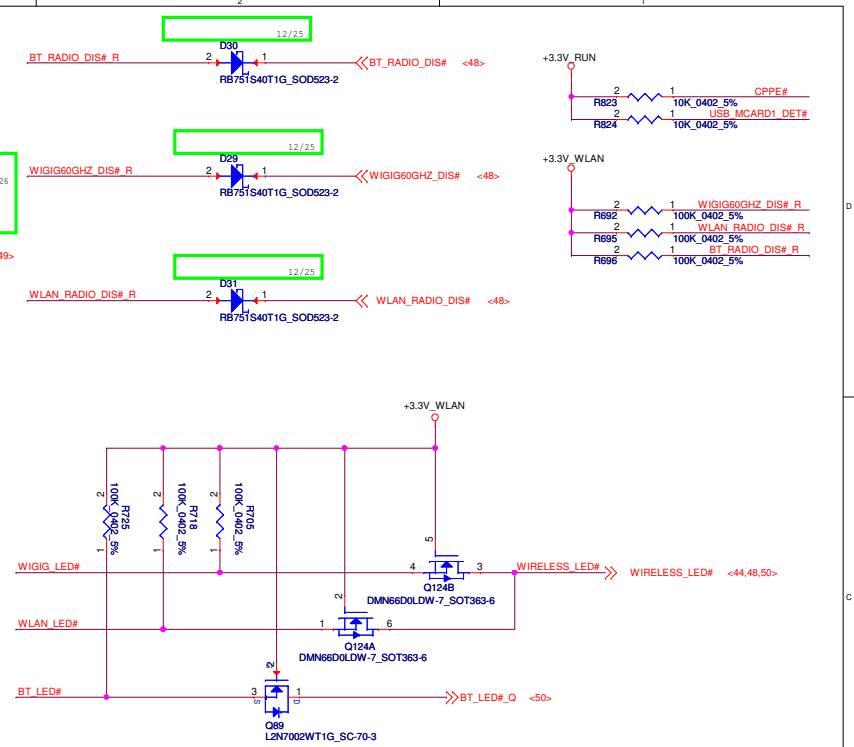
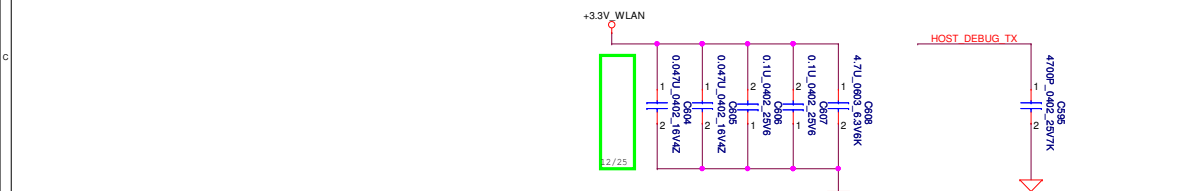
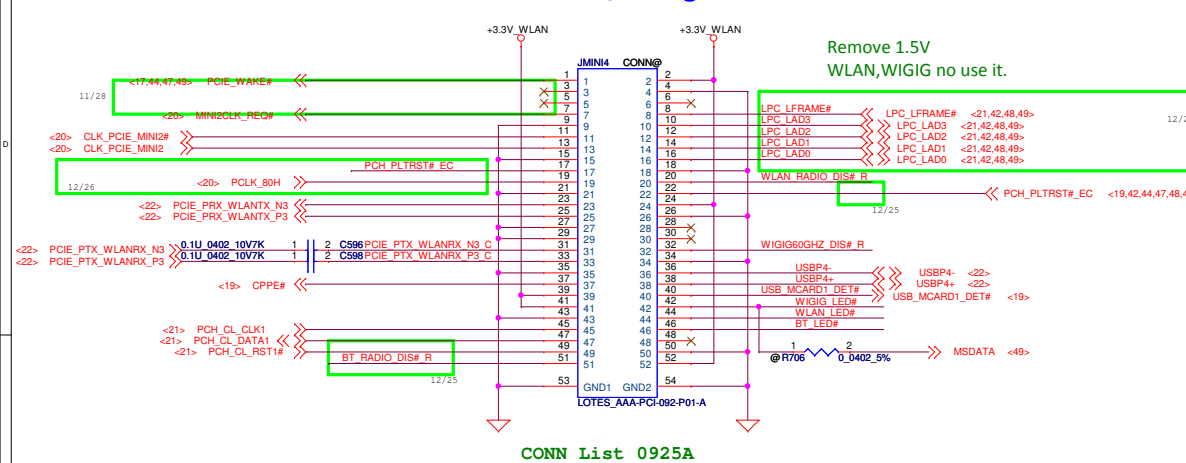
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Size	Document Number	LA-9771P	
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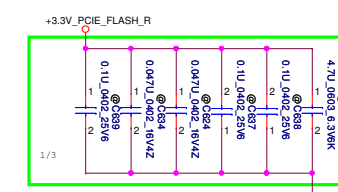
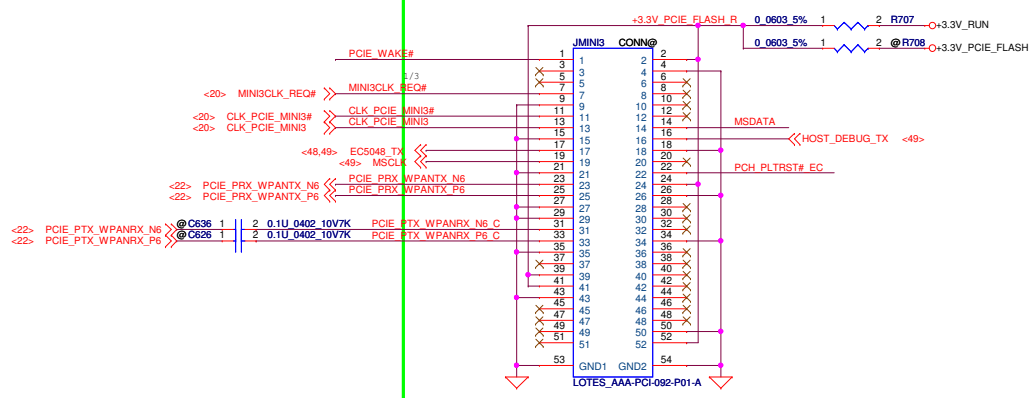
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Mini WLAN/WiGig H=4



Pink Pather H=5.2



CONN List 0925A

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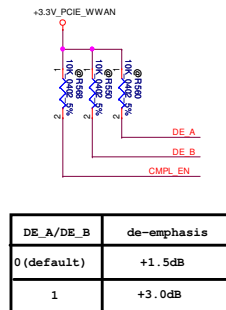
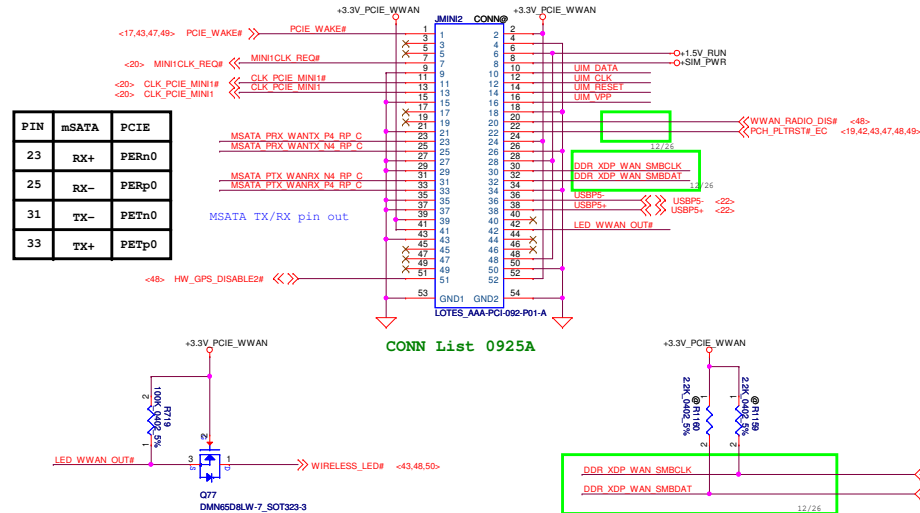
Mini Card-1/2

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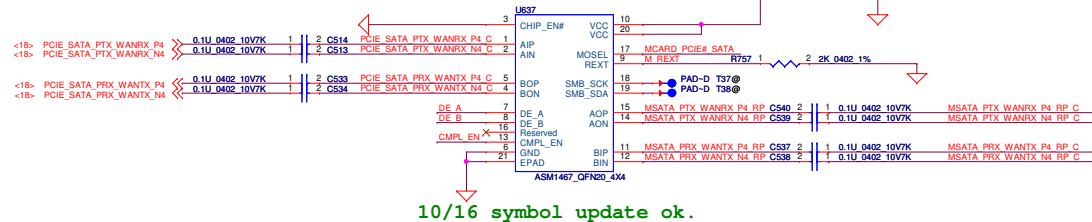
Mini WWAN/GPS/LTE/mSATA



CHIP_EN#	Funtion
0	Normal mode
1	power down mode

MCARD_PCIE_SATA# (GPIO16)	FLEX IO 13
L	PCIE
H	SATA

PCIE/SATA Repeater



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Mini Card-2/2

File: LA-9771P

Size: Document Number

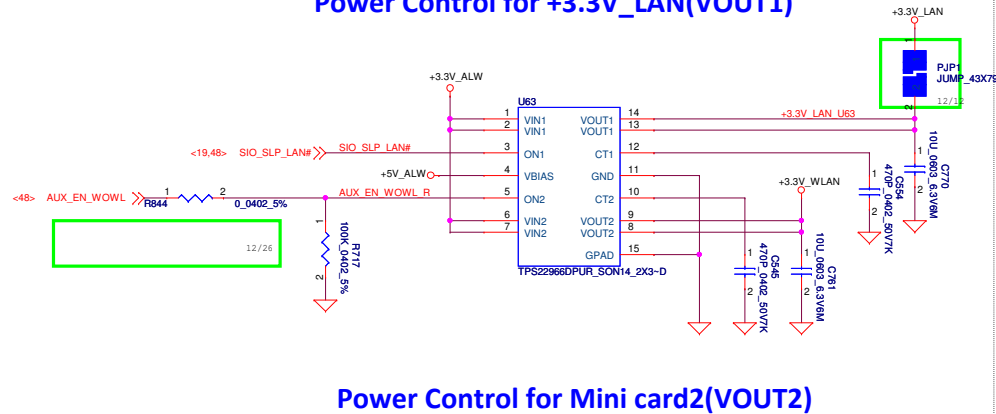
Date: Tuesday, January 15, 2013

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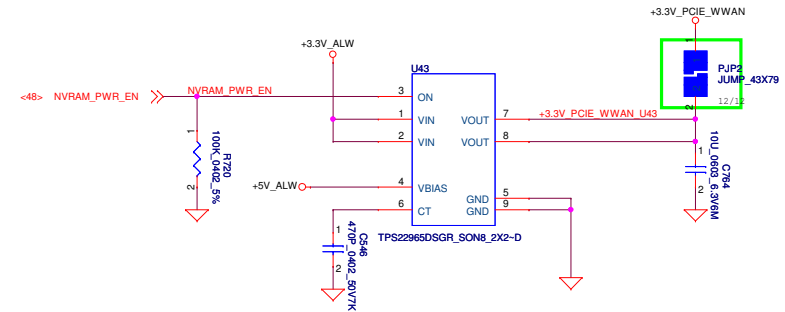
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Power Control for +3.3V_LAN(VOUT1)

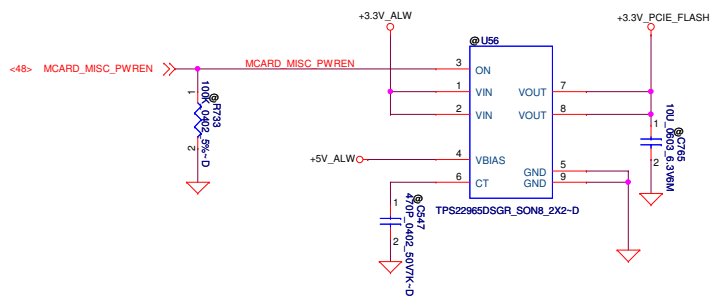


Power Control for Mini card2(VOUT2)

Power Control for Mini card1



Power Control for Mini card3



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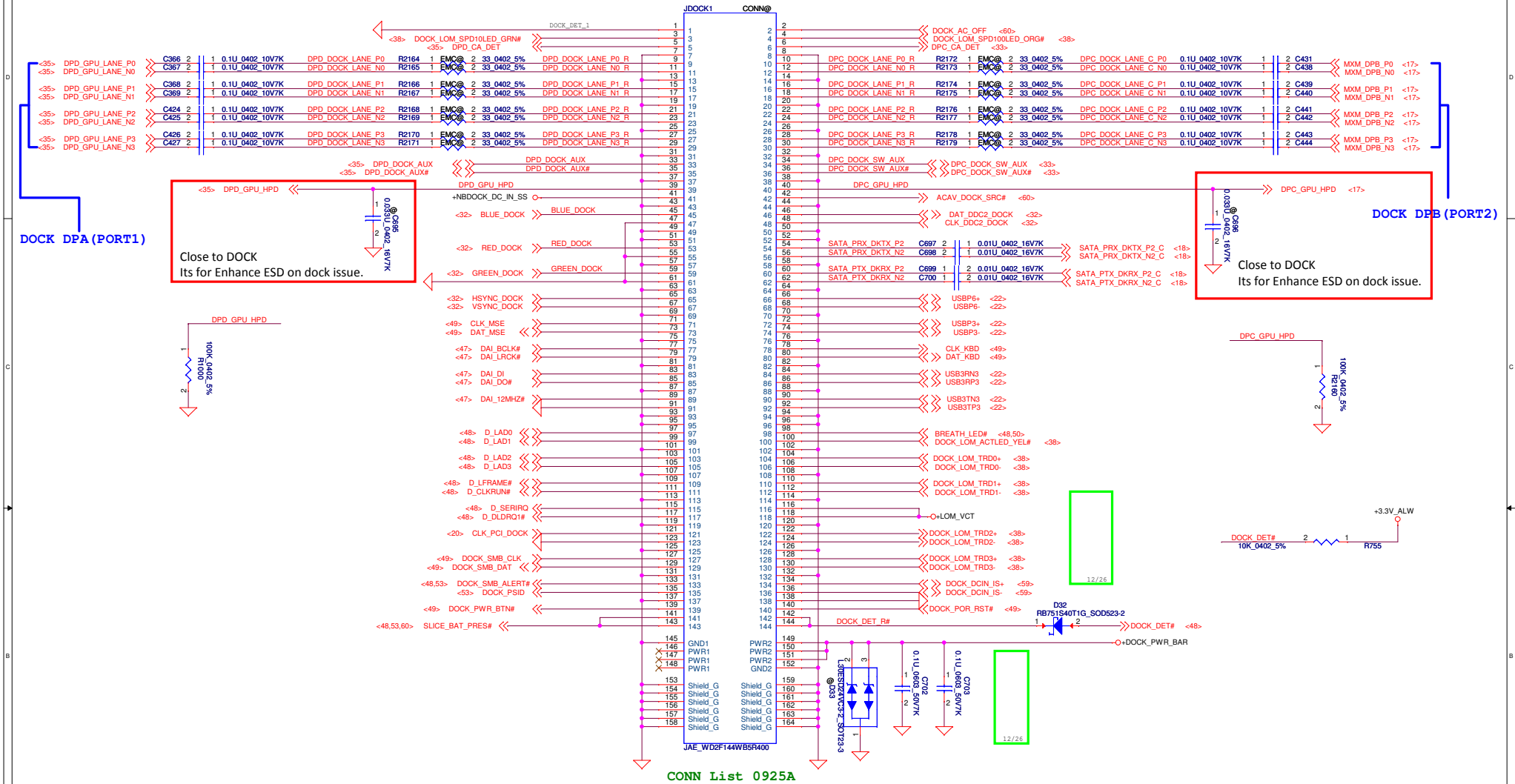
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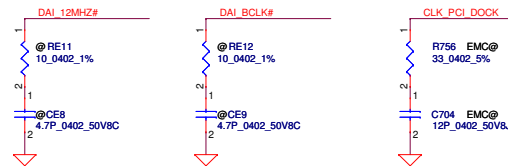
Mini Card PWR

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EMI request add 33ohm for DOCK DVI signals.



CONN List 0925A



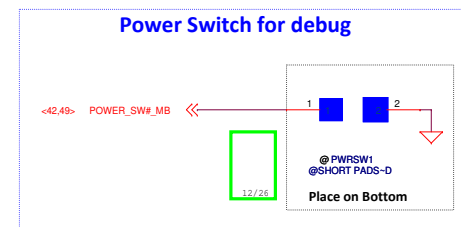
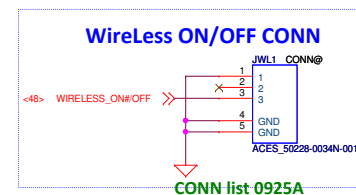
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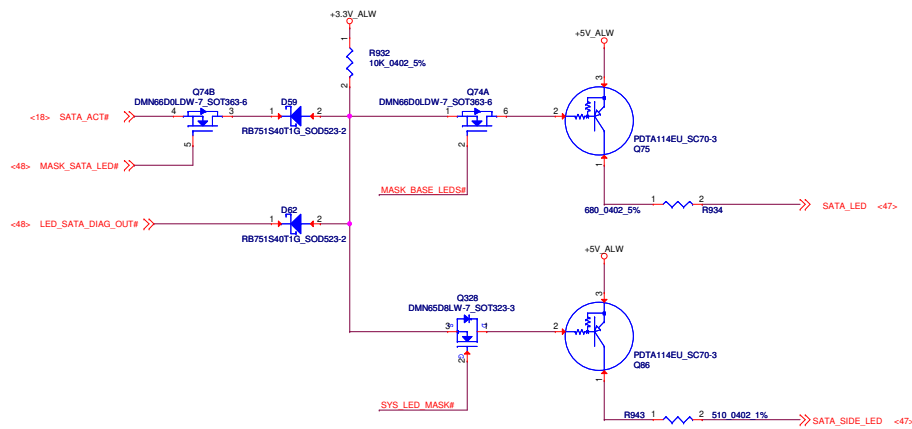
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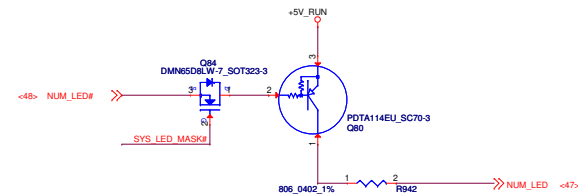
WWW.AliSaler.Com



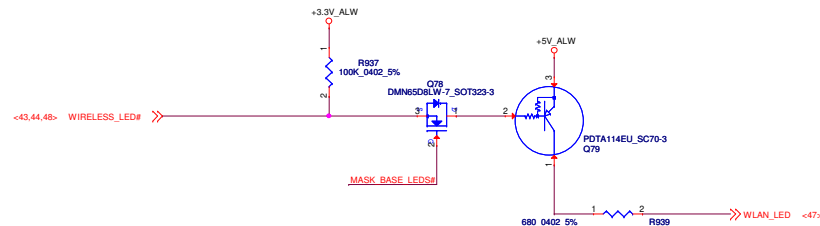
HDD LED



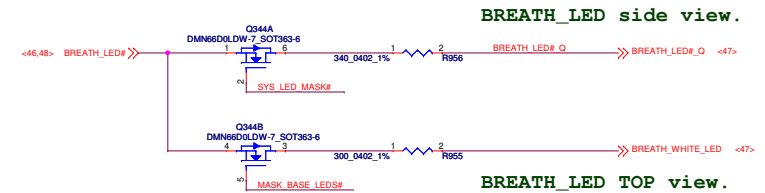
NUM LED



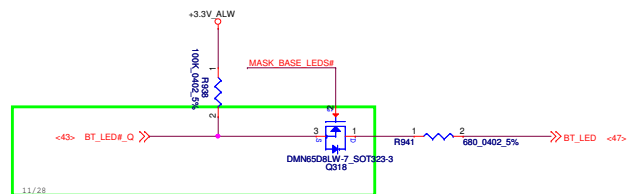
WWAN/WLAN LED



Breath LED



BT LED

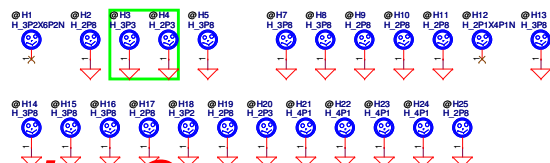


LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark

- FD1
- FIDUCIAL MARK-D
- FD2
- FIDUCIAL MARK-D
- FD3
- FIDUCIAL MARK-D
- FD4
- FIDUCIAL MARK-D



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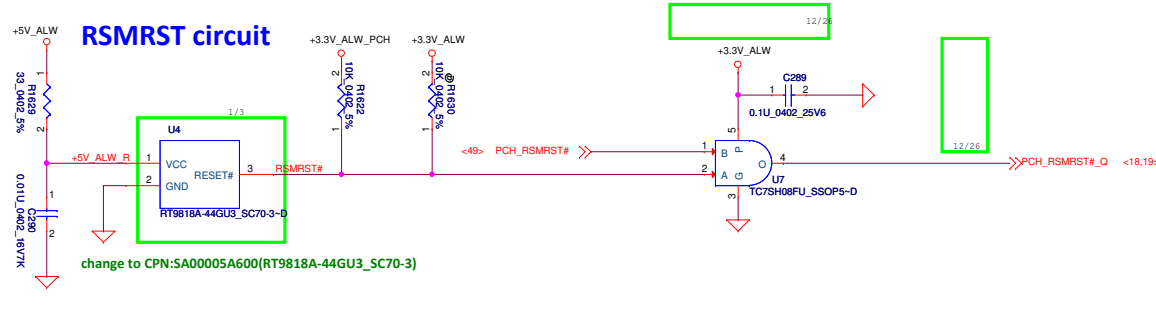
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PAD & Standoff & LED

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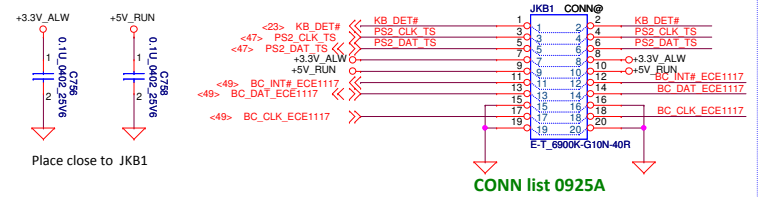
RSMRST circuit



BlueTooth

11/28

Keyboard



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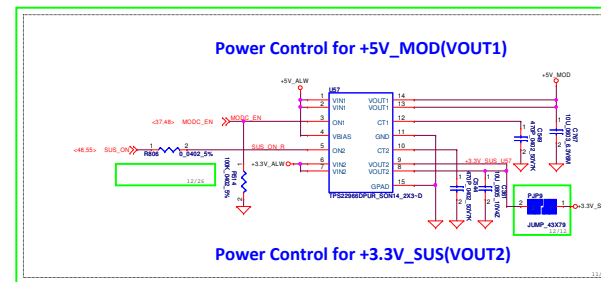
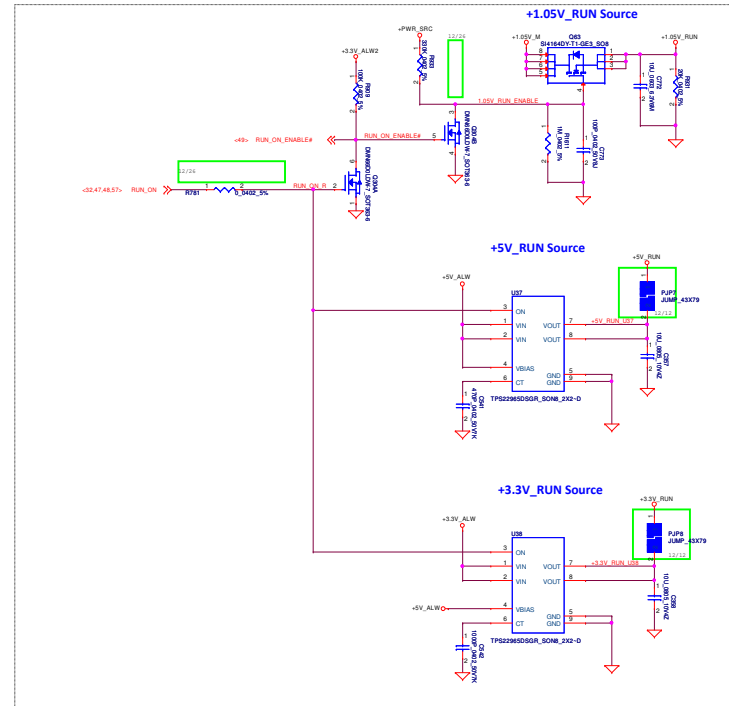
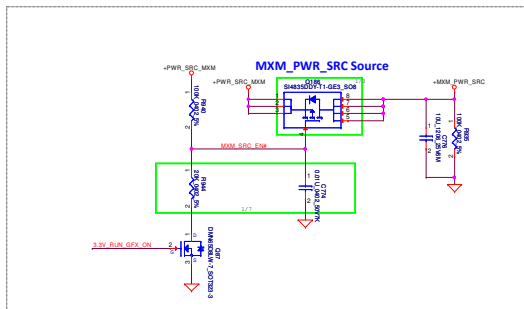
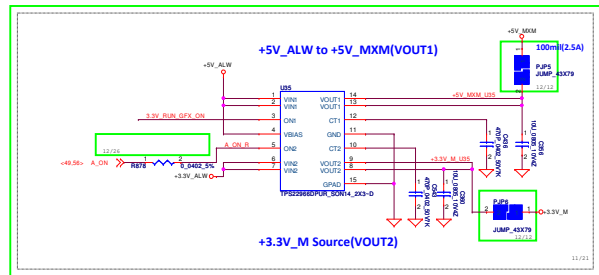
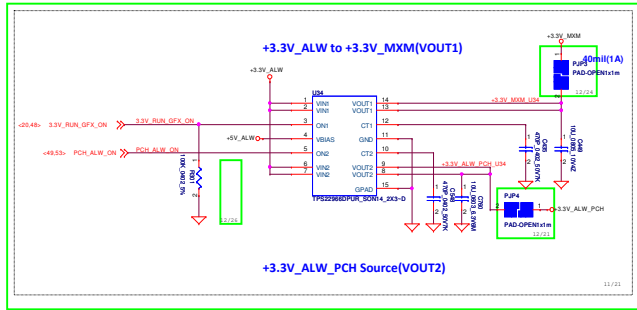
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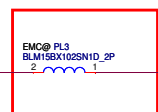
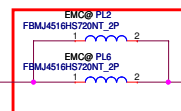
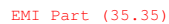
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Size	Document Number	LA-9771P	
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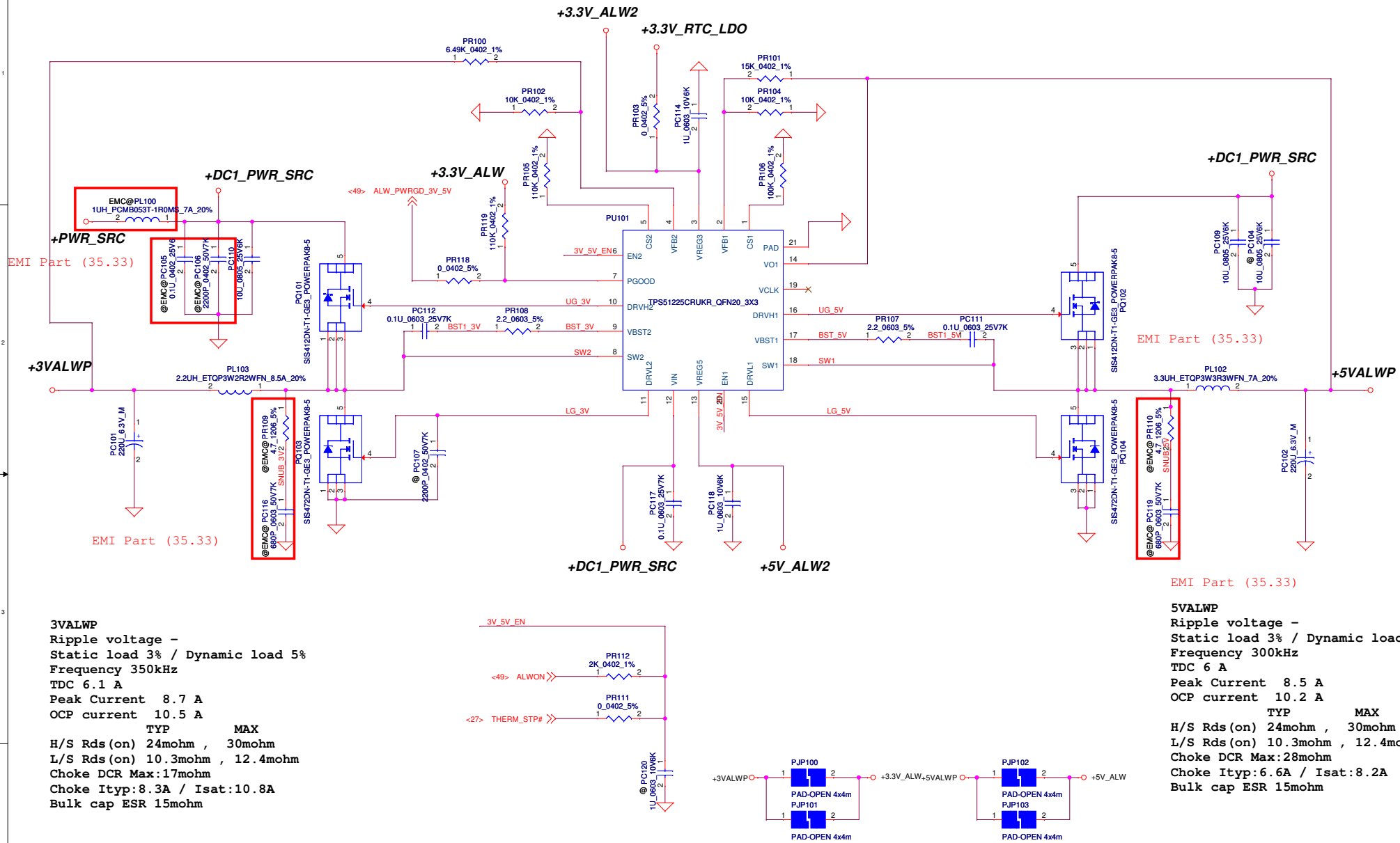
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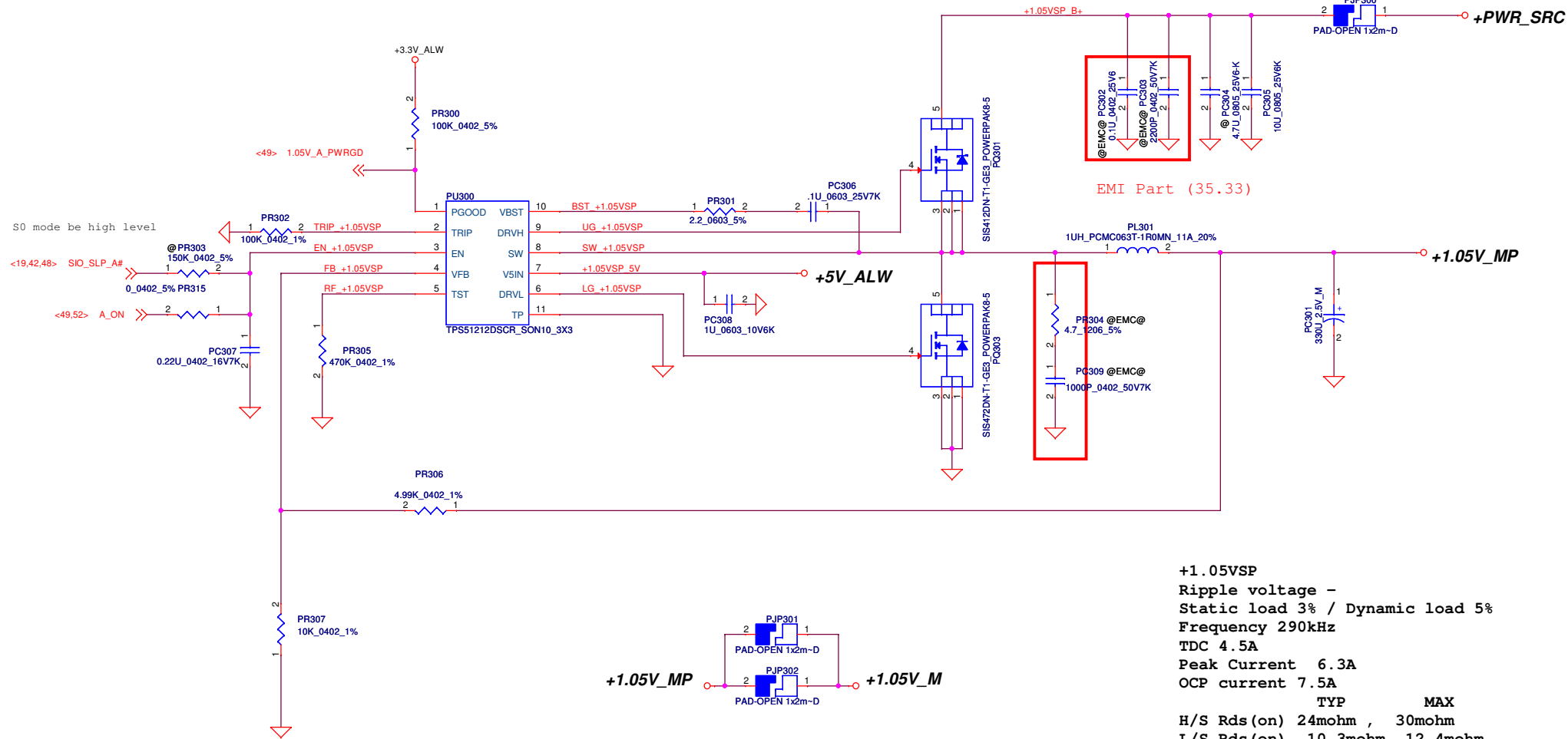
Rev 0.2







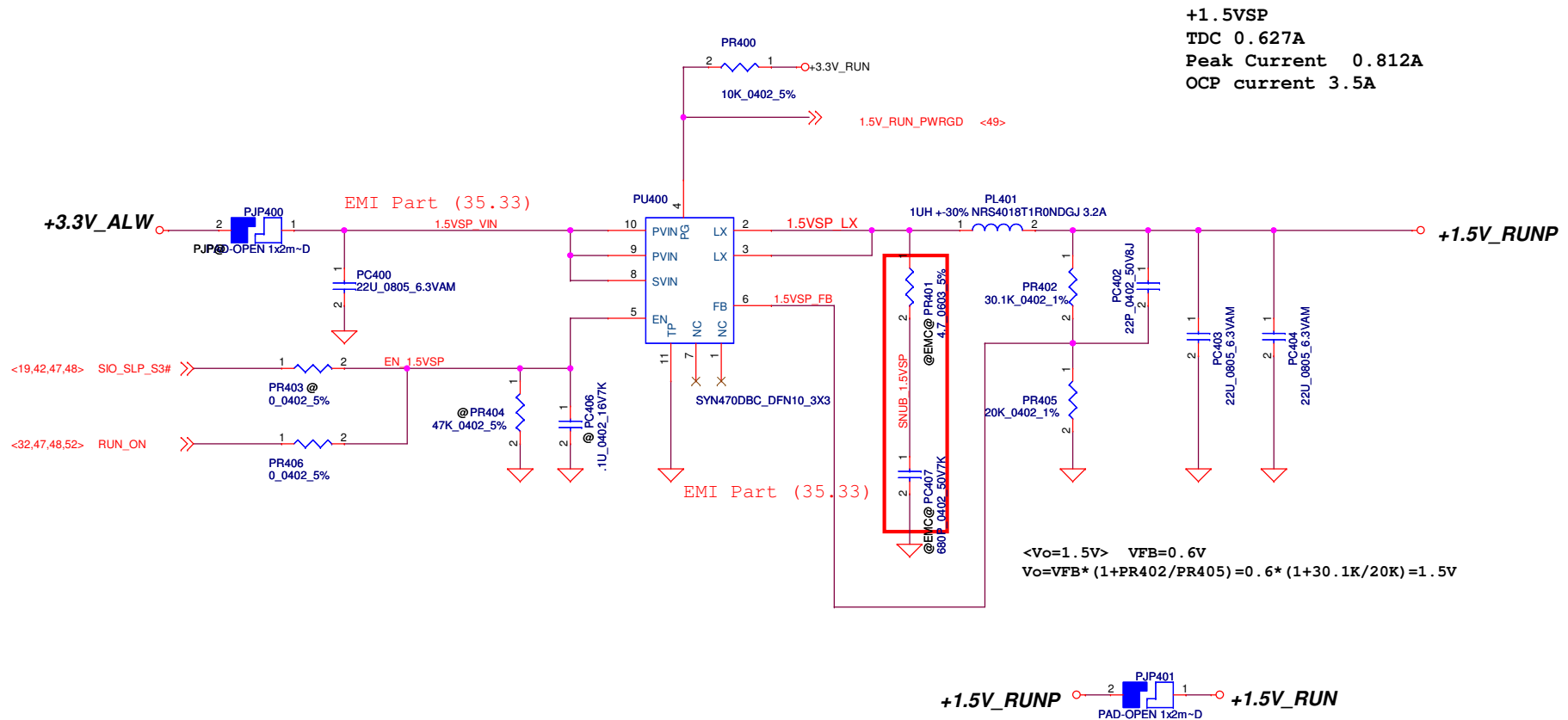
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Issued Date	2012/01/17	Deciphered Date	2013/01/16	Title	PWR-3VALWP/5VALWP
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+1.05VSP
 Ripple voltage -
 Static load 3% / Dynamic load 5%
 Frequency 290kHz
 TDC 4.5A
 Peak Current 6.3A
 OCP current 7.5A

TYP MAX
 H/S Rds(on) 24mohm , 30mohm
 L/S Rds(on) 10.3mohm , 12.4mohm
 Choke DCR 11mohm
 Choke Ityp:11A / Isat:14.5A
 Bulk cap ESR 17mohm

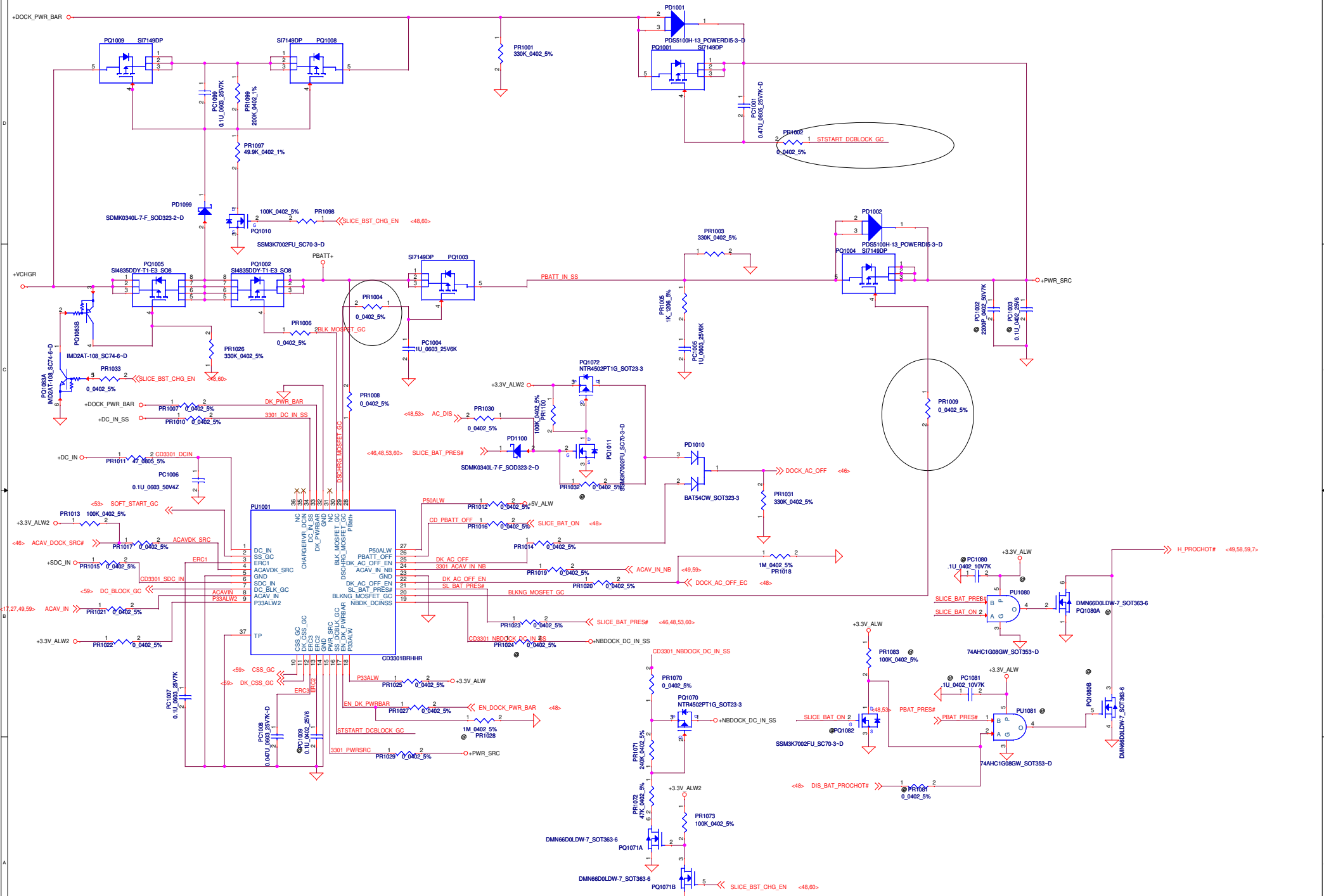
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Title			
PWR-1.5VSP			
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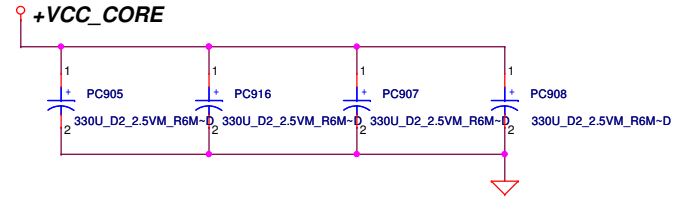
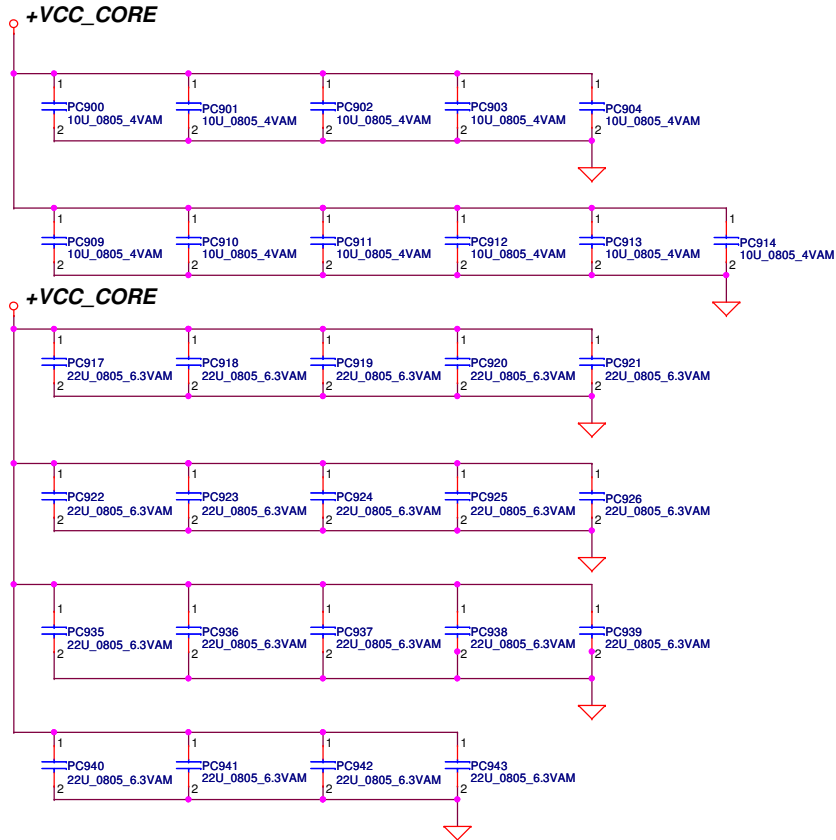
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Based on PDDG rev 0.7 Table 5-1.



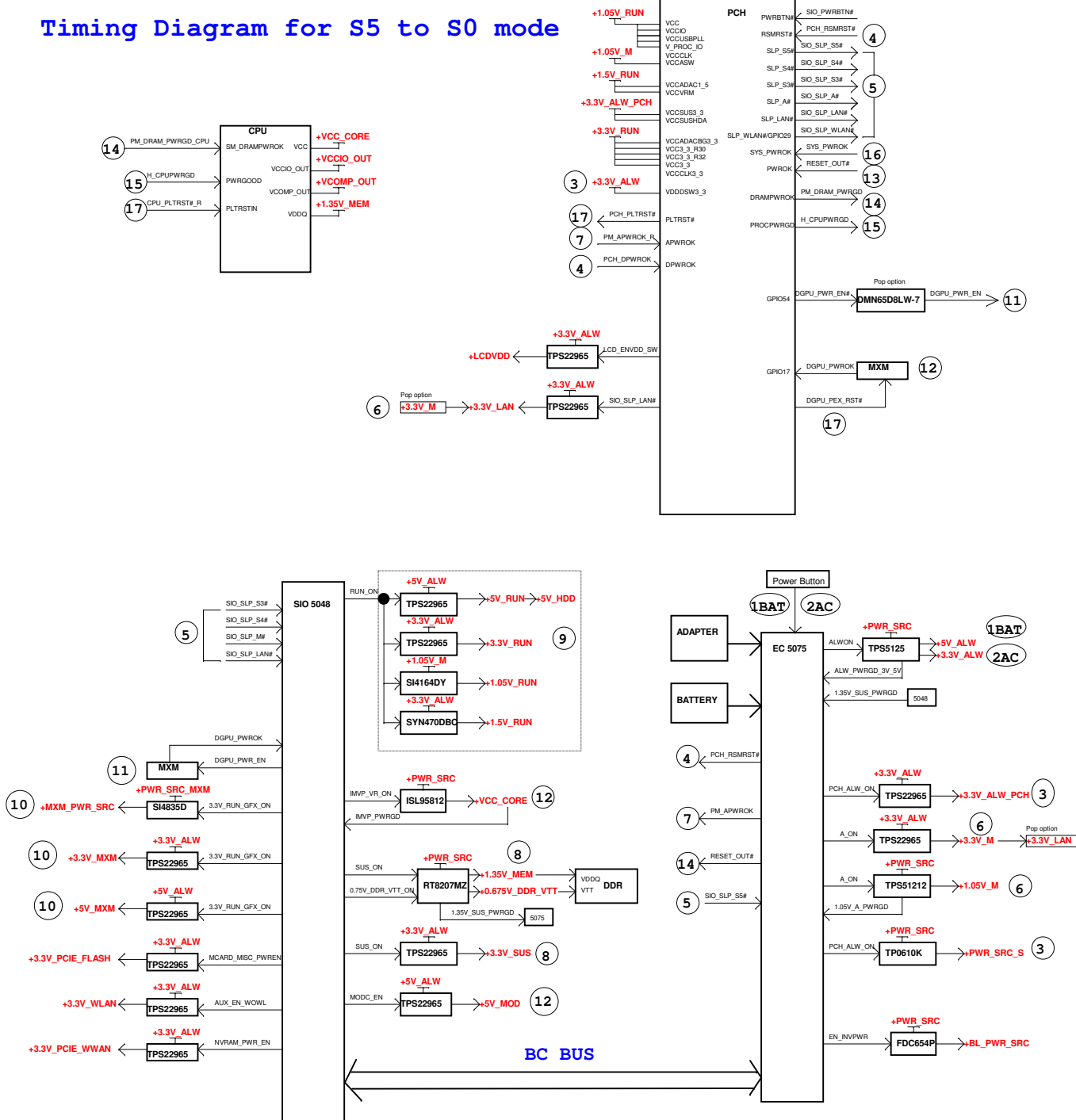
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Timing Diagram for S5 to S0 mode




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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	38	HW	10/30/2012	DELL	Both EC_WAKE# and LAN_WAKE# to be connected to GPIO27 of PCH	pop R556.	X01 (0.2)
2	30	HW	11/21/2012	compal	Q24,U46(ECE5048)burned out issue on SSI build IPQC test.	Change JLVDS1.5~JLVDS1.15 pin define.	X01 (0.2)
3	30, 49	HW	11/21/2012	compal	add BIST support(I2C solution) for QHD+ panel	add Q6,R161,R162. remove R239,R228. change MXM_EDP_HPDP to JEPWR1.1 and BS of R839,R840 to 2@.	X01 (0.2)
4	23	HW	11/21/2012	compal	intel ME Crypto TLS cipherher suite with confidentiality.	pop RH37 and change to 1Kohm.de-pop RH62.	X01 (0.2)
5	45, 52	HW	11/21/2012	compal	component reduce plan-merge load sw from 1ch/1chip to 2ch/1chip.	merge (U63,U42); (U57,U41); (U34,U36); (U35,U40) depend on actual layout routing.	X01 (0.2)
6	9, 50, 49, 13 14, 15, 16	HW	11/22/2012	compal	SSI memo	change QC6 to SB00000QO00. de-pop C778,R1986,R1197,R1118,CD80,CD22,CD44,CD66,CD88	X01 (0.2)
7	22, 42, 43, 50 51	HW	11/28/2012	DELL	BT 4.0 USB module dropped for ARD REV1.2	change Q318 to SOT323 package remove R2207,R33,R34,R702,C600,R707,R724,R694,D28,C748,C754,C753,R904, R1133,R1134,JBT1	X01 (0.2)
8	20, 22, 43, 45 48	HW	11/28/2012	DELL	Pink Panther dropped for ARD REV1.2	change JMINI3 PWR from +3.3V_PCIE_FLASH to +3.3V_RUN remove C765,C547,R733,U56,C636,C626,C625,C635,C639,C634,C624,C637, C638,C633	X01 (0.2)
9	30	HW	11/30/2012	compal	PS8723B EQ table error	correct EQ table follow vendor suggestion.LL=9.5dB,LH=13dB,HL=4.5dB,HH=7.5dB.	X01 (0.2)
10	13, 14, 15, 16	HW	12/11/2012	INTEL	DDR Layout routing.	follow CRB DQ0~DQ63 distribution(DIMM1,DIMM3) and boardfile routing. DIMM2,DIMM4 depend on DIMM1,DIMM3 routing to define DQ0~DQ63.	X01 (0.2)
11	45, 52	HW	12/12/2012	compal	battery life measure.	add PJP1,PJP2,PJP5~PJP9(JUMP_43X79), PJP3,PJP4(JUMP_43X39)	X01 (0.2)
12	30	HW	12/12/2012	compal	panel sequence(LCDVDD tr=T1,PWR_SRC tr= T12)	change C555 from 0.1uF to 0.01uF,C297 from 1000pF to 0.47uF.	X01 (0.2)
13	18, 20	HW	12/12/2012	compal	crystal EA	change CH4,CH5 from 18pF to 10pF;CH13,CH14 from 18pF to 12pF.	X01 (0.2)
14	41	HW	12/14/2012	DELL	Charger current change to 1A.	change U2 to SLG55594AVTR(SA00006L600).	X01 (0.2)
15	42	HW	12/19/2012	compal	APS pin define change for DG1.5	change JAPS1.7 to POWER_SW#_MB,remove R19,R31,R29.	X01 (0.2)
16	7	HW	12/19/2012	INTEL	VCCIO_OUT 6KHz noise in shark Bay 2-chip platform	change CC66 from 0.1uF to 1uF and pop it.	X01 (0.2)
17	49	HW	12/19/2012	compal	Board ID	change R875 from 240Kohm to 130Kohm.	X01 (0.2)
18	30, 32, 48	HW	12/19/2012	ESD	ESD EA	remove D87,D13,D10,D11,C749,C750.	X01 (0.2)
19	19, 48	HW	12/20/2012	compal	Deep Sleep feature support	pop R802,RH101,RH75,RH131;de-pop RH79,RH91.	X01 (0.2)
20	11, 14	HW	12/20/2012	compal	1.35v decoupling cap reduce	de-pop CD34,CC36,CC35,CC40,CC169,CC166,CC165,CD36,CC38,CC33, CC42,CC37,CC41,CC163,CC170,CC171,CC168,CC164	X01 (0.2)
21	41	HW	12/20/2012	compal	Layout routing	Swap D15 D+,D-; L39 D+,D-.	X01 (0.2)
22	14, 16, 30, 52	HW	1/7/2012	compal	inrush current EA	add R944(20Kohm),change C774 from 2200P to 0.01U for +MXM_PWR_SRC. de-pop CD37,CD38,CD82.CD83 for +0.675V_DDR_VTT. de-pop C300 for +3.3V_RUN glitch during turn on +CAMERA_VDD.	X01 (0.2)
23	48	HW	12/27/2012	DELL	AC_DIS# polarity is inverted.	AC_DIS# signal change to AC_DIS,due to it's high active for "Peak Shift".	X01 (0.2)
24	23, 42	HW	1/2/2013	compal	USH/B drop O2 solution in X5.	remove netname"SMART_DET#".	X01 (0.2)

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25	18, 51, 52	HW	1/3/2013	compal	replace X1 code component for LOAD BOM.	change U4 to SA00005A600,QH2 to SB501380020,Q186 to SB00000FF00.	X01 (0.2)
26	38	HW	1/3/2013	compal	LAN EA.	change R570,R575~R581(0ohm) to L63~L70(12nH).	X01 (0.2)
27	20, 22, 43, 45 48	HW	1/3/2013	DELL	Add Pink Panther and reserve them.	add R707,R708,C765,C547,R733,U56,C636,C626,C639,C634,C624,C637,C638,C633	X01 (0.2)
28	47	HW	1/3/2013	compal	USBP0+/- layout routing.	swap USBP2+/- from JIO1.20/JIO1.18 to JIO1.18/JIO1.20.	X01 (0.2)
29	23, 42	HW	1/7/2013	compal	reserved routing SP_TPM_LPC_EN on PCH GPIO22 for GPIO MAP3.0	add R2189,RH209,depop RH208,change netname PCH_GPIO22 to PCH_TPM_EN.	X01 (0.2)
30	44	ME	1/4/2013	compal	connector List 1217A	change JSIM1 from T-SOL_159-1000302600 to T-SOL_159-1000302602 (SP011212271).	X01 (0.2)
31	43	HW	1/7/2013	compal	modify netname and cap placement.	add +3.3V_PCIE_FLASH_R on R708.1 and change C639.1 net to +3.3V_PCIE_FLASH_R.	X01 (0.2)
32	50	ME	1/7/2013	compal	screw hole change.	change H3 to 3P3,H4 to 2P3.	X01 (0.2)
33	13, 16	HW	1/8/2013	compal	DFX repair issue.	pop CD80,depop CD14.	X01 (0.2)
34	30	HW	1/8/2013	compal	change main source circuit design for phase in LCDVDD PWR SW 2nd source.	add R709,depop C555.	X01 (0.2)
35	37	HW	1/8/2013	compal	R796.1 PWR plane error.	change R796.1 PWR plane from +3.3V_ALW to +3.3V_ALW PCH.	X01 (0.2)
36	19, 48	HW	1/8/2013	compal	reserve non-DS3 function circuit	add R802,RH101,RH79,RH91	X01 (0.2)
37	42	HW	1/9/2013	compal	TPM chip change version to DX4A12.	change U39 to SA00004WQ40(AT97SC3204-DX4A12-ABF).	X01 (0.2)
38	23	BIOS	1/10/2013	compal	let EC set U46.B3(MCARD_PCIE_SATA#) as OD to save power same as Goliad/salado.	change RH226.2 from GND to pull up +3.3V_RUN	X01 (0.2)
39	30, 40, 41	EMI	1/11/2013	compal	EMI request change USB2.0 choke.	change L10,L39,L41,L51 to DLW21HN900SQ2L(SM070001N00).	X01 (0.2)

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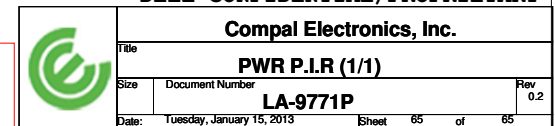
			
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1	55	PWR	11/29/2012	COMPAL	For 1.35V selector	Unpop PR225, PR224, PR218, PR220, PR217, PR211, PR222, PR223, PC217 PQ205, PR221, PC220, PR216, PR219, PC219, PQ204, PR213, PC216	X01
2	54	PWR	11/29/2012	COMPAL	For 3.3V OCP setting	Change PR105 to 90.9K	X01
3	57	PWR	11/29/2012	COMPAL	For 1.5V output voltage setting	Change PR402 to 30.1K, PR405 to 20K	X01
4	54	PWR	11/29/2012	COMPAL	For 3.3V/5V output voltage setting	Change PR102 and PR104 to 10K 1%	X01
5	58	PWR	11/29/2012	COMPAL	Change better Vcore MOSFET	Change PQ500, PQ502, PQ504 to CSD87350Q5D	X01
6	53	PWR	12/11/2012	COMPAL	Main source have x1 code	Change PQ1, PQ1070 to SB00000H500	X01
7	53	PWR	12/11/2012	COMPAL	Main source have x1 code	Change PU1 to SA00003DN00	X01
8	59	PWR	12/11/2012	COMPAL	For part count reduction	Combine PQ707, PQ708 to SB00000DH0L	X01
9	56	PWR	12/11/2012	COMPAL	For part count reduction	Unpop PC304, change PC305 to SE00000QK00	X01
10	55	PWR	12/11/2012	COMPAL	For part count reduction	Unpop PC208, change PC207 to SE000008L80	X01
11	55	PWR	12/20/2012	COMPAL	Unite to same part number	Change PQ1, PQ1070 to SB000007900	X01
12	58	PWR	12/20/2012	COMPAL	For EMI test	Pop PC515	X01
13	55	PWR	12/21/2012	COMPAL	For cost down	Change PL201 to SH000004S00, PL701 to SH00000PO00	X01
14	60	PWR	12/26/2012	COMPAL	For Japan's Energy star	Add PQ1072, PQ1011, PD1010, PR1030, PD1100, PR1100, PR1031, PR1032	X01
15	60	PWR	12/26/2012	COMPAL	For boost charger behavior	Add PR1026, PQ1083	X01
16	59	PWR	12/26/2012	COMPAL	For current sense accuracy	Change PR706=33.2ohm, PR708=6.8ohm, PR713=12.1ohm, PR715=20ohm	X01
17	58	PWR	01/03/2013	COMPAL	For Vcore compensation	Add PR558=5.1Mohm, PC509=820pF	X01
18	58	PWR	01/03/2013	COMPAL	For EMI request	Pop PC516=470pF	X01
19	59	PWR	01/07/2013	COMPAL	Unite to same part number	Change PD703 to SCS0340L010	X01
20	53	PWR	01/07/2013	COMPAL	Change to small size bead	Change PL3 to SM01000MB00	X01
21	59	PWR	01/08/2013	COMPAL	Refer to E5	Change PR737.1 to +3.3V_ALW2	X01

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